# OVERVIEW OF FE-B OPERATION AND PERFORMANCE

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**Provide overview of operational aspects of FE-B, including register definitions, known bugs, etc.**

**Review measurements on FE-B to indicate what we know about the performance, particularly of the front-end.**

- More details at: **http://www-atlas.lbl.gov/pixel/doc/Electronics.html**

# Measurements on FE-B Front-end

## Some measurements can best be done with dedicated test chip:

- Allows examining internal signals to better understand performance of individual blocks
- Allows switching known quantities on inputs: injecting known leakage current and applying known capacitive load
- Allows more detailed studies of performance as a function of DAC settings to find performance optimum

## Some measurements can best be done in complete array:

- Do not really know the capacitive environment seen by a real front-end
- Real leakage currents may have large variations between channels
- System effects, not in test chips, may also affect results

## Following plots are a mixture of these two sources

# Pinout of FE-B

## Comments on pinout details:

- P14 = Shield is connected to the M3 shield over the digital readout logic in the active pixel matrix. This pin needs to be connected to either AGnd or DGnd.
- P24, p25 = VCom, VThr are not connected in FE-B
- P26-p33 = I1 through I8 are connected to the DACs in the order the DACs appear (I1 is connected to DAC0, etc.). Lab tests indicate that both for single chips and for complete modules, no decoupling is required on these nodes.
- p42-43 = MON_HIT is the positive polarity, differential HitBus (p42 = MON_HITn) for the high-threshold discriminator. It should be terminated in 500-600 ohms for normal LVDS operation.
- p44-45 = MON_TIME is the positive polarity, differential HitBus for the low-threshold discriminator. It should be terminated in 500-600 ohms for normal LVDS operation.
- p46 = MON_AMP is the output for the test pixel buffer amplifier, suitable for driving a high impedance connection only.
- p47 = MON_REF is the output of the internal current reference in voltage form. Lab tests indicate that this node does not require decoupling. With standard supply voltages, it should sit slightly above 1.0 V.

# Command Register in FE-B

- Definitions of common bits in Command Register (first 16 bits):

  **1 SoftReset:** perform reset of digital section of chip only (pulse)

  **2 ClockSelect:** enable clock to shift data into Pixel Register (level)

  **4 ClockDAC:** enable clock to shift data into shadow DAC Register (level)

  **8 ClockGlobal:** enable clock to shift data into shadow Global Register (level)

  **16 WriteMask:** strobe Select bits into local Pixel Mask Register (pulse)

  **32 WriteDAC:** strobe shadow DAC Register into actual DAC Register (pulse)

  **64 WriteGlobal:** strobe shadow Global Register into actual Global Register (pulse)

  **128 ReadDAC:** load DAC Register into shadow DAC Register (pulse)

  **256 ReadGlobal:** load Global Register into shadow Global Register (pulse)

  **512 EnableAnalog:** enable analog charge injection based on Select bits (level)

  **1024 EnableDigital:** enable digital hit injection based on Select bits (level)

  **2048 EnableHitBus:** enable HitBus output based on Mask bits (level)

  **4096 EnableBuffer:** enable test pixel preamplifier buffer (level)

- Definitions of private bits in Command Register (second 8 bits):

  **1 EnableSingle:** enable single discriminator mode (level)

  **2 WriteTDAC:** write threshold DAC settings from Global Register into local latches (pulse)

  **4 WriteLatency:** transfer latency value from Global Register into Greycode generator (pulse)

- Note “pulse” implies the internal signal returns one CCK after LD ends. The five Enable bits must remain set in each command to preserve the desired action.

# Details of Command Register operation:

- Command Register uses CCK*LDBar for clock, other registers use ChipSelect*Clockxxx*CCK for clock. ChipSelect is set after address recognition in the command register and returns low after LD returns low.
- Even “dataless” commands require always at least one CCK while LD is high (more is OK, as the MCC cannot issue less than 2 CCK under LD)
- The implementation of the “pulsed” mode is not quite according to spec, since it requires an additional CCK rising edge after LD goes low in order to bring the internal signal low. In general, the internal signal is for a latch, so the latch sees the new value (becomes transparent) immediately, but doesn’t truly latch the result until the next CCK. Hence, it can be operated without the extra CCK.
- The implementation of readback has a similar flaw, in which the first data bit returned after LD goes high is undefined, and the interesting data bits come back as the [second] to [n+1] bits from the register. Hence, always issue an extra CCK during readback, and ignore the first bit after LD goes high.
- Due to loading of the output bits from the Global Register, the TDAC load does not allow loading of the TDACs for the whole chip at the same time. Typically, we load the chip in smaller groups of 10 pixels per column. Note the loading technique is totally different from that of FE-A: here you load a TDAC value into the Global Register, and when the command WriteTDAC is given, this value is loaded into all Selected pixels.

# DAC Register and Adjustments in FE-B

**CINDAC (DAC0)**: Preamplifier bias adjustment

- Adjusts preamplifier bias, but load bias and source follower bias have a fixed ratio to the preamp bias. The default (64) gives about 5-6 μA in the input transistor.

**FPDAC (DAC1)**: Feedback current adjustment.

- A setting of 20 gives about 0.5 μs return to baseline time for a 20 Ke input.

**ABSDAC (DAC2)**: AC-coupling bias adjustment

- Adjusts AC-coupling stage bias. This has a small effect on the undershoot for the AC-coupling circuit, but barely changes shaping performance of the front-end. A setting of 20 gives little undershoot.

**D1DAC (DAC3)**: Diff-amp bias adjustment.

- This both changes the speed of the diff-amp, and also changes its interaction with the global threshold adjustment. The default is about 3.5 μA, but 5 μA gives much better performance (96 instead of 64 counts).

**THBDAC (DAC4)**: Global threshold adjustment.

- This adjusts the baseline (reference point) for the diff-amp. Large values give low thresholds. The range and slope of the adjustment depend on D1DAC.

**DLDAC/DTDAC (DAC5/DAC6)**: Level/Time discriminator bias adjustment

- This adjusts the bias of the discriminator transistors when they are switched on. It affects the threshold (threshold difference) slightly. DTDAC has a large range with some impact on the timewalk. DLDAC has a smaller range.

**THADAC (DAC7)**: TDAC step size adjustment

- This adjusts the size of the TDAC steps, and should be matched to the initial dispersion at fixed TDAC value. Under normal conditions, a setting of 100 works well for 300e of un-tuned threshold dispersion, and the adjustment is linear.

## Register conventions:

- Note DAC0 is the first register after the DI, whereas DAC7 is the last register before DO. The bit string is loaded such that the first bit into the chip is the MSB of DAC7 and the last bit in is the LSB of DAC0.

## Default settings of DACs:

- For most measurements, the standard values include:

  CINDAC = 64, ABSDAC = 20, D1DAC=96, DLDAC = 80, DTDAC = 64

  FPDAC is varied from 1 to 40, but usually at 5 or 20

  THBDAC is varied from 1 to 100 or more

  THADAC is usually in the range of 80 to 140

- This gives a power consumption of about 40 μW/pixel and good performance.

# Global Register

## Register bit definitions for Global Register:

- It is a 24 bit register, where the first bit clocked in should be the MSB (bit 23) and the last bit in should be the LSB (bit 0).
- **Bit 0-6:** Latency value in beam crossing units, where 0 implies a latency of 128 crossings. Follow with WriteLatency to reload and start Greycode generator.
- **Bit 7-15:** column pair mask field. Not connected in FE-B.
- **Bit 16-18:** DO MUX field, controlling what is multiplexed from the DO pin:

  0 = Command/Address Register connected directly (reset condition)

  1 = Pixel Register

  2 = DAC Register

  3 = Global Register

  4 = Event Data

- **Bit 19-20:** Phi Clock control, controlling the frequency of the column clock (the chip operates correctly for 5 and 10 MHz):

  0 = 40 MHz

  1 = 20 MHz

  2 = 10 MHz

  3 = 5 MHz

- **Bit 21-23:** TDAC setting to be loaded into pixels with WriteTDAC

  the value 0 is the minimum threshold, whereas 7 disconnects the TDAC

# Procedure used for Register loading:

- For the Global Register, first a ClockGlobal is used to transfer data into the shadow register, then the WriteGlobal is used to transfer this data into the actual register. Values are checked using ReadGlobal followed by ClockGlobal.

# Procedure used for TDAC loading:

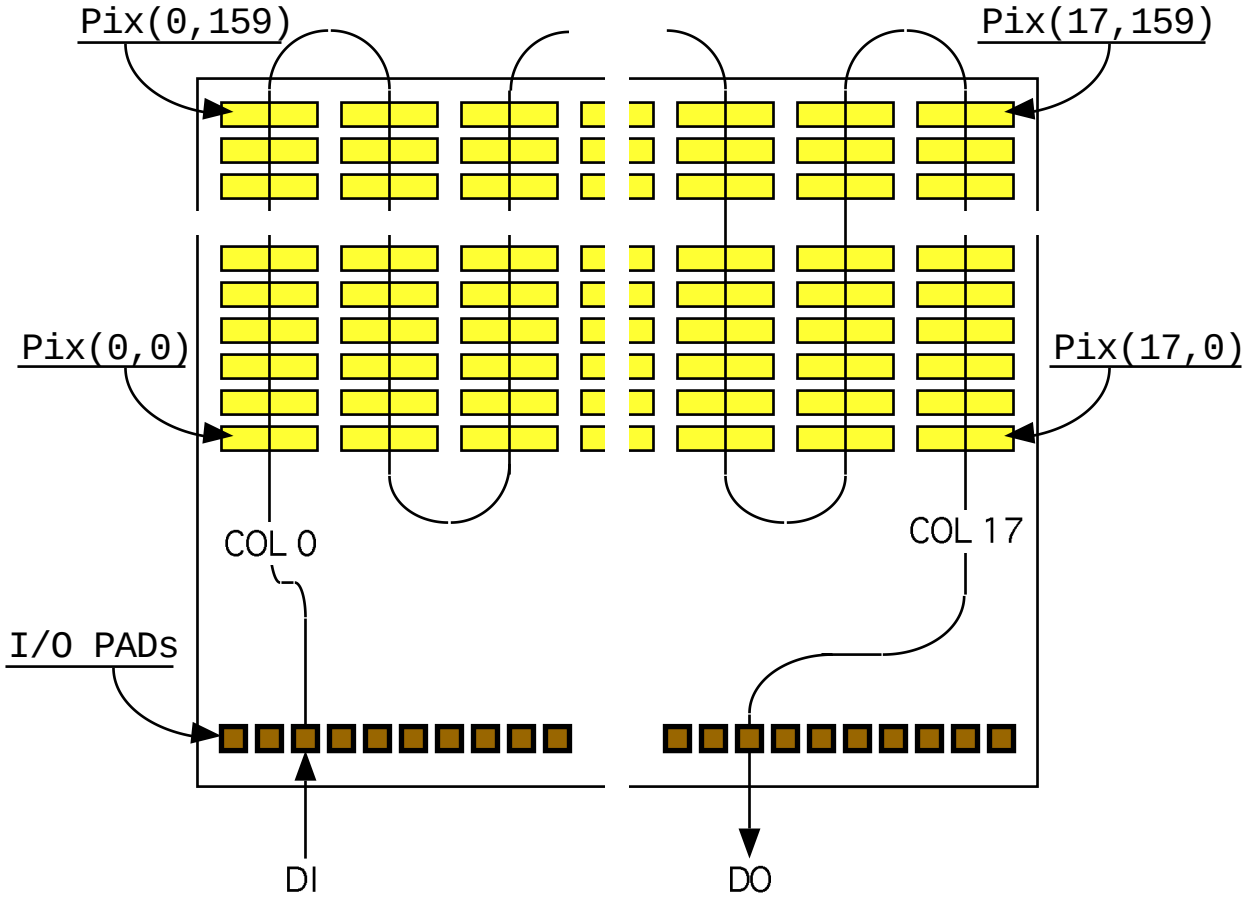
- Loop over 16 groups of 10 pixels per column (row 0-9, row 10-19, etc), and for each group:
- Loop over the eight possible values for the TDAC.
- For each group of 180 pixels, and each one of eight possible TDAC values, the Global Register is loaded with the relevant TDAC value, the Pixel Register is loaded with the bits to enable loading of the TDAC value from the Global Register into the Selected pixels, and finally the WriteTDAC command is executed to store the value into the three FF in the pixels.

# Procedure for Latency setting:

- Any time the Latency value is changed in the Global Register, it is necessary to restart the Grey counter with the WriteLatency command before the new value takes effect.

# Pixel Register

- For this register, Select=1 is active (enables charge injection) and Mask=1 is enabled (enables readout and HitBus).
- Order of bits in the register is given by the figure in the Demonstrator specifications:



# Example Command Sequences

## To test the DAC Register:

- ClockDAC to load DAC settings
- WriteDAC to latch the settings in the actual DAC Register
- ClockGlobal to set the DO MUX for readback of the DAC Register
- WriteGlobal to latch the data into the actual Global Register
- ClockDAC to flush out contents of DAC shadow register
- ReadDAC to transfer the actual DAC Register value into the shadow register
- ClockDAC to transfer this data out of DO

## To write a new Latency value:

- ClockGlobal to load new Latency value
- WriteGlobal to update the data in the actual Global Register
- WriteLatency to restart the Grey generator

## To write a new mask set into the pixels:

- ClockSelect to load appropriate pattern into the Pixel Register
- WriteMask to transfer these bits into the Mask latch in each pixel

# Reset Behavior

## When the external RSTb pin is pulsed:

- XCK must be present, and the duration should be at least 250 ns:
- Internal ChipSelect will be cleared
- Command Register will be cleared to zero
- DAC Register latches are set to '01000000', or 1/4 of full scale. This should correspond roughly to the nominal values for the biasses
- Global Register latches are all set to 0
- Pixel Register and Mask are not affected

## When a SoftReset is issued:

- Will reset the digital circuitry in the readout chip, including restarting the Greycode generator (requires a new WriteLatency afterwards).

## When a SYNC is issued:

- Will reset the read and write pointers to the Trigger FIFO to clear all pending events.

# Calibration Options

## Three different options are supported by the FE chip itself:

- **EnableDigital** set: digital hit injection, in which the Strobe input is sent directly into the pixel control section (the middle of the pixel), and the output from the pixel front-end is ignored. The injection is controlled by the Pixel Register in the same way as analog injection. This offers the possibility of creating hits with a known TOT even if the front-end is not operational (for example if the detector is not biased).
- **EnableAnalog** set: analog charge injection, in which the Strobe input operates a chopper circuit in the chip periphery to generate a fast step on the nominal 10 fF injection capacitor with height given by the VCal analog input. The pixel circuitry for this operation uses a transmission gate to connect the chopped VCal value to the injection capacitor, followed by a FET switch to AGnd. If a pixel is Selected, the transmission gate is closed and the grounding switch is open. Otherwise, the transmission gate is open and the grounding switch is closed, preventing even parasitically coupled charge to be injected by this path.
- Neither set: in this case, the chopper is left in its normal Strobe-off state (VCal passes through), and it is possible to inject an externally-created VCal pulse directly to the pixels which are Selected. For non-calibration operation, this would normally be the Strobe state, and the Select register would be all zero, preventing any coupling of noise on VCal into the pixel front-ends.

# Known Features and Problems

## Readout timing problem:

- Due to a race condition in the horizontal sparse scan, after 5 column pairs, data starts to get lost. Normally, the first hit from each column pair is reset and lost, but in the last column of the chip, there is an additional hit lost. We normally operate the chip with the readout for the last 4 column pairs disabled (read out 1600 channels), to avoid any confusion. This problem can be fixed by focussed ion beam modifications (two cuts and two jumpers per die), but this is not practical for large numbers of die.

## Minor logic errors:

- For Latency = 0, the stretching of the overflow flag is not performed correctly, effectively giving it zero length, and so it is never latched for transmission in the EOE word. Hence, buffer overflows are not detected properly for this latency value.
- For latency not equal to zero, the algorithm used for the TOT subtraction in the case where the subtracted value would be negative, is incorrect. The result is that large TOT values (greater than the L1 latency) can be seen in the data. The correct value is obtained in this case by subtracting the present latency setting (the correct coding is TOT = MOD(TOT,LATENCY)).

## TDAC Load problem:

- There is a loading problem for the 3-bit TDAC value in the Global Register. If one tries to set this value into too many pixels in the matrix at the same time, the load fails. The workaround is to load the array in 10 steps (16 pixels per column at any one time). This appears to work very reliably.

## Internal chopper problem (???):

- In early testing, it was observed that there was a non-statistical fluctuation in the behavior of the FE near threshold when performing a threshold scan. This manifested itself as S-curves which oscillated wildly between 0% and 100% hits seen in the transition region. Subsequent testing has not confirmed this problem. Now, a threshold offset of about 1.1Ke relative to external injection is observed.

## Column arbitration limitation:

- The present column arbitration unit that sits between the column pair and the end of column buffers gives priority always to the left-most column of the pair.
- If there is a large amount of activity in the column pair, it is possible to lose essentially all of the hits in the right-most pair, while retaining most of the hits in the left-most pair.
- Future implementations will give priority to the column that was not the one most recently read out, to make hit losses more uniform.

# After-pulsing problem:

- In the present readout architecture, if the LE of a new hit arrives in a pixel when the backend of that pixel is still busy transferring the previous hit, and the TE arrives when the backend of the pixel is no longer busy, then the hit is not lost. However, the LE latch information will not be updated, while the TE information is updated. The result will be what appear to be two hits on the same pixel in the same crossing, with the second one having much larger TOT. This is a side-effect of the fact that the hit detection circuitry in the pixel back-end is not truly edge-sensitive, but is only level sensitive.
- It has also been observed (on both the Hitbus and the full digital readout), that under some conditions, there is “digital crosstalk” in the pixel. In this case, the presence of hits on many column pairs in the chip will cause many pixels to re-fire. This activity is associated with the operation of the column clock (it some cases, when slowing the column clock to 5 MHz, one can see HitBus pulses appearing at the 5 MHz frequency). It is almost certainly due to a combination of several things:

  → The column clock activity is synchronous in all column pairs on the chip, so operation of all column pairs at the same time, for example when calibrating, enhances the problem

  → The shield over the digital parts of the column pair is not well-connected to the chip periphery due to limited routing space available on FE-B.

→ The transfer of data in the column pair causes synchronous, full-swing CMOS activity on 22 bits of data bus in the column pair. Because of its length, this data bus has a relatively large capacitive coupling to the shield.

→ The effect is usually only visible with detectors which include large conductive nets (examples are the SCP common p-stop design and the SXT window-frame design). Presumably this improves the ability of the shield on the electronics side to couple charge into the pixel implants on the sensor side.

- The result is that when a given pixel sees this digital crosstalk, and re-fires, it is quite likely that a second hit will be generated in the same crossing. One will therefore see events in which one pixel produces two hits associated with the same trigger. This causes problems for the threshold fitting software, and is in general a source of extra “noise hits”. However, even in the chips with the worst after-pulsing behavior (such as the first SCP-01 assembly), testbeam operation appears normal, because simultaneous hits on many column pairs are required to trigger after-pulsing.
- The after-pulsing problem is being addressed in future versions by using low-swing signals for transmitting the hit information to the end of column buffers.
- The problem of recording multiple hits in one crossing can be solved by making the initial hit detection circuitry in the pixel edge sensitive. In this case, the pixel back-end would simply ignore hits in which the leading edge occurred while the pixel was busy. However, if the “digital crosstalk” problem is eliminated or strongly suppressed, this clean hit acceptance behavior, which costs area in the pixel back-end, will be somewhat less important.

# Trigger FIFO Overflow problem:

- There is a restriction on the maximum number of events which can exist in the FE-B at any given time (that is the number of accepts for which events have not yet been completely transmitted). This limit is related to unique labeling of the events with an internal 4-bit trigger number as well as to the 16-entry size of the trigger FIFO which stores information on each active event.
- It has been observed than when sending an excessive number of triggers to the FE-B chip, it is possible to sometimes enter a “stuck” mode in which the chip will continue to transmit EOE words forever, even in the absense of additional L1 triggers. A hard reset to the chip is required to return to normal operation.
- This situation can happen in HitBus readout mode when the chip has many noisy pixels, since the PLL imposes no deadtime between successive triggers beyond the “non-overlapping” requirement that a new trigger will not be issued until a time of one L1 latency has passed.
- In future versions, this will be dealt with in the FE chip by simply disabling the L1 trigger from entering the readout control logic if the trigger FIFO is full. This will lead to the loss of data, but will not lead to mis-behavior of the type mentioned above. This situation should never occur in full MCC mode, since the MCC will throttle the incoming triggers. Note however that the present MCC simply stops transmitting data as soon as it receives more than 16 active events, and ignores all further triggers until it receives a reset.

# Signals induced in preamps during Pixel Register operation:

- If a FE-B chip is operated close to its minimum threshold in “readout all” mode (where the readout of all channels is enabled, such as for a source scan using the Hitbus), then extended periods of pixel firing can be observed following operation of the Pixel Register, for example when the chip is initially configured.
- In extreme cases, such as a module with poor LV decoupling, this can make the module very difficult to operate in a stable manner.
- For future versions of FE chips, it is strongly recommended that the pixel control logic is operated off of the DVdd supply, and not the AVdd supply as in FE-B. This should significantly reduce the sensitivity to these problems.

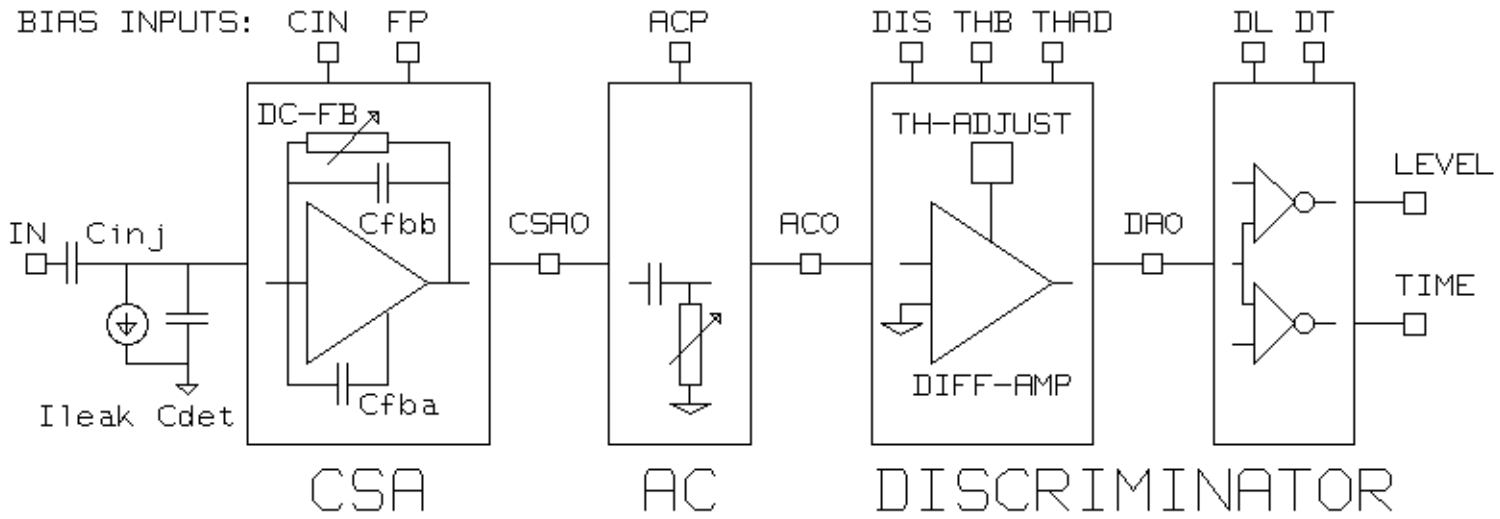
# Power Consumption

## Observed power consumption on three supplies:

- Normally operate supplies at DVdd = 3.5V, AVdd = 3.5V, AVcc = 1.75V. The chip operates correctly at 3.0/3.0/1.5V, but has not been extensively tested at these voltages. This low voltage operation is not expected to be realistic for irradiated rad-hard chips, so we choose the higher voltage. The preamp, because of cascoding design, etc. would probably not operate well at 3V post-rad.
- On AVcc supply: power consumption is totally controlled by the setting of CINDAC, and the default setting of 64 gives about 5.5 μA of current. The total current under normal conditions is about 16 +/- 1 mA for 2880 pixels.
- On AVdd supply: power consumption is dominated by CINDAC, D1DAC and Hitbus buffering. The nominal observed current is about 38-40 mA for the chip, of which about 15 mA is related to the Hitbus buffering, and 25 mA is related to the front-end itself. The total AVcc plus AVdd is about 170 mW, but only about 120 mW should be expected in a final chip.
- On DVdd supply: power consumption is about 20-25 mA on single-chip card after subtracing off LVDS conversion chips on PC board. This is less than 100 mW.
- For a 16-chip module, the observed consumption is about 250 mA on AVcc, 700-750 mA on AVdd, and 400-450 mA on DVdd (including the MCC chip). The total module consumption is then about 4.5W, roughly within the ATLAS budget.

# Front-end Design

## Block Diagram:



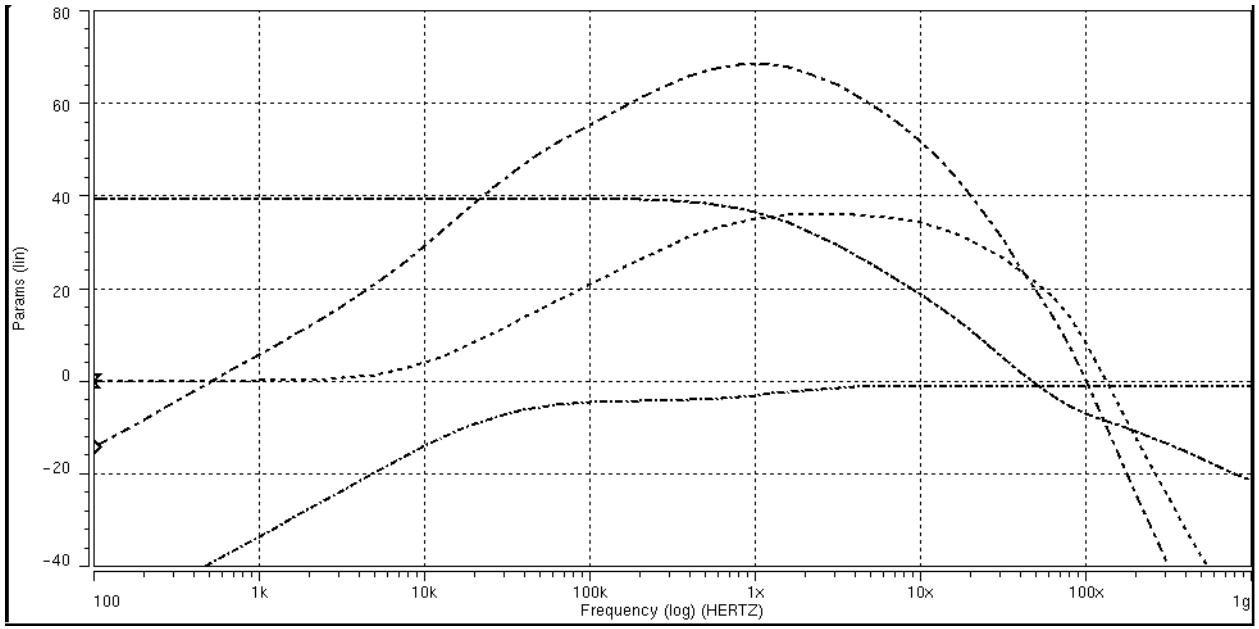

- Diagram indicates the four basic blocks, and the eight DAC-adjustable biasses

## Features:

- Fast, high-gain preamp with DC-feedback based on CPPM concept
- AC coupling stage with non-linear element to provide minimal undershoot
- Slower diffamp stage to minimize crosstalk effects
- Dual-threshold discriminator with good delta-threshold matching

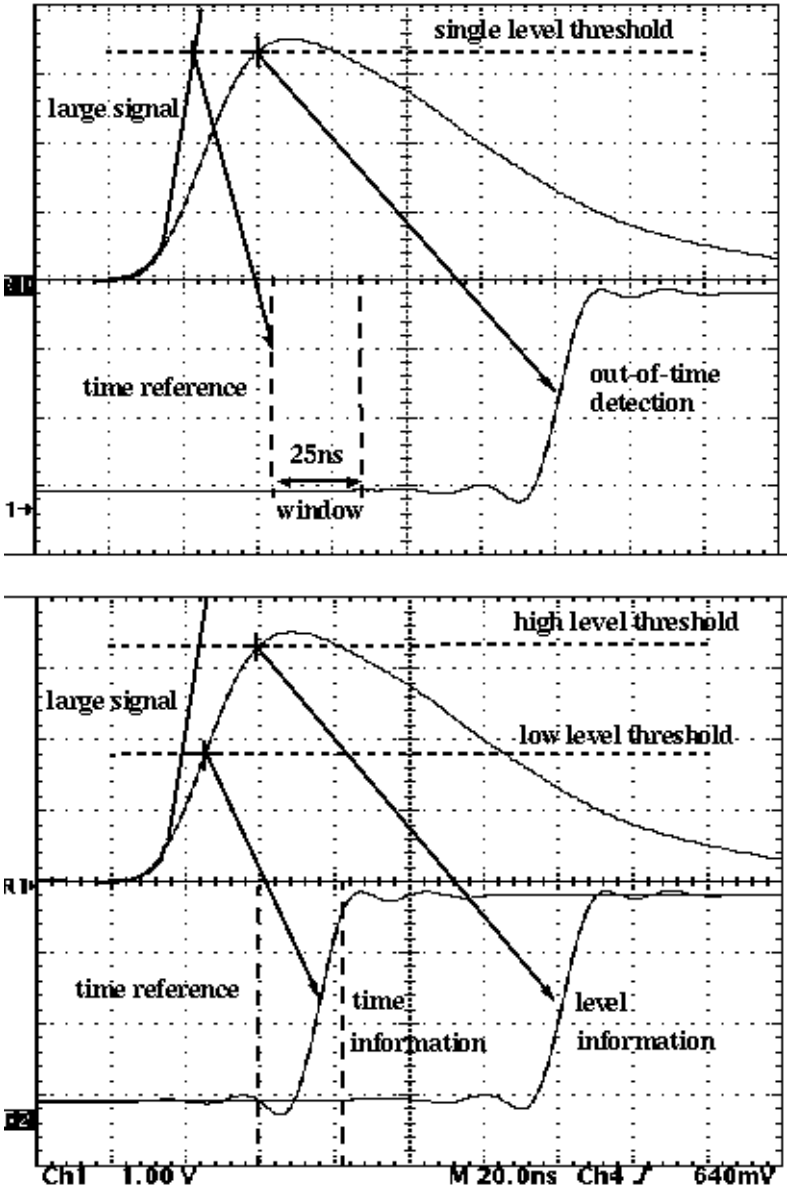
# Dual-threshold design:

- Slower second stage to suppress fast bipolar crosstalk signals relative to real input signals:




- Overall transfer function peaks about 1 MHz. Preamplifier peaks at several MHz, but diffamp rolls off above 1 MHz, suppressing faster signals.
- This approach will increase the timewalk, in exchange for suppressing the crosstalk signals. The dual threshold design gives the freedom to eliminate out-of-time hits. The diffamp must still be fast enough to allow setting a sufficiently low in-time threshold.

# Why two thresholds ?

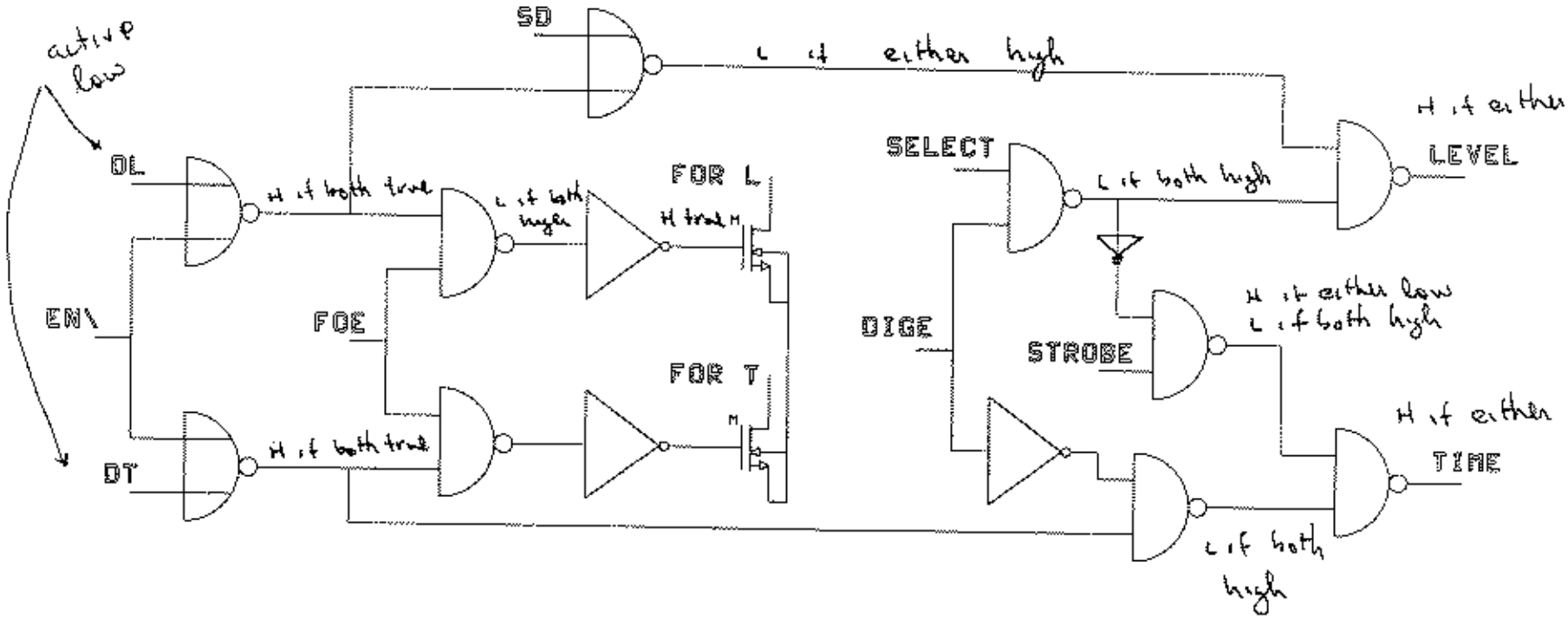



- With a single discriminator threshold, there is always a window in pulse height where the output pulse will be out of time.
- The threshold must be set low to allow good timewalk performance, but this will produce many “noise” hits
- With two thresholds, the threshold separation can be adjusted so that any out of time hit on the low-threshold discriminator does not fire the higher threshold, suppressing all out-of-time hits
- In addition, this design gives the flexibility to separately adjust the low threshold for good timewalk and the high threshold for acceptable “noise” occupancy

# Control Logic

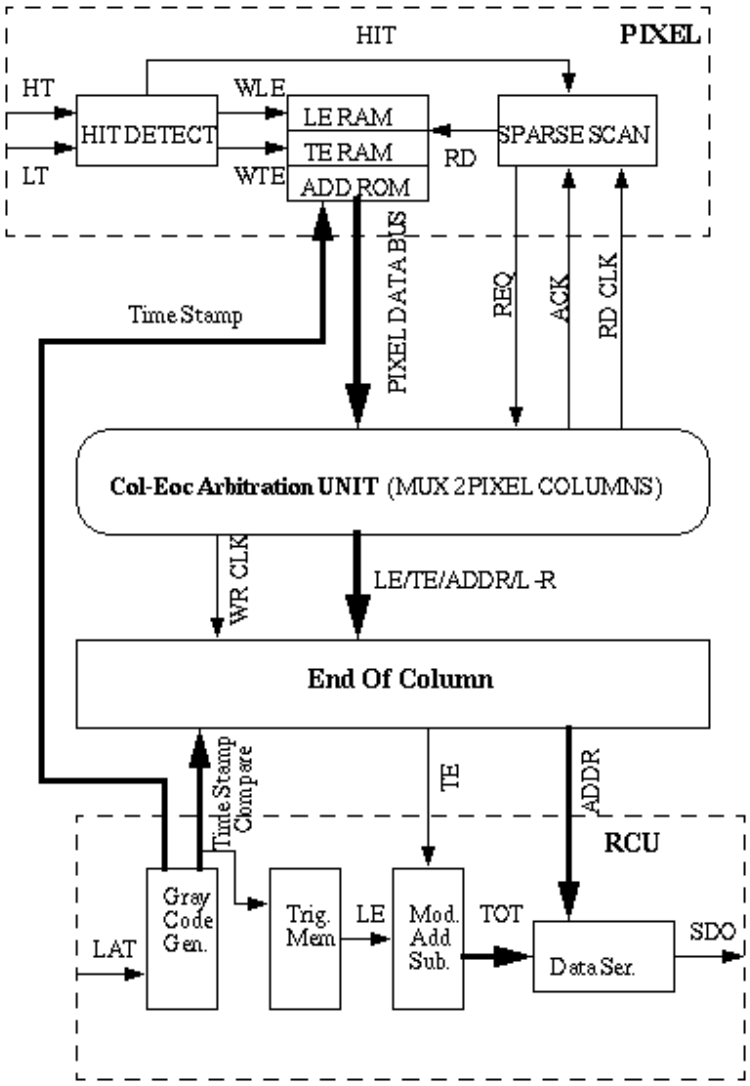
## The control section is located in the middle of the pixel, and includes the following logic:

- This section also includes the Pixel Register and the Readout FF that is used to control readout.
- Note the use of German symbol for OR (lines extending through AND symbol)
- Note also that for historical reasons, this logic is operated off of the AVdd supply.



# Readout Architecture

## Timestamp architecture:




### Pixel logic:

- A coincidence between low and high threshold inputs generates a hit. The leading and trailing edge timing are given by the low threshold discriminator.
- Timestamp (7-bit Greycode beam crossing number) values are recorded for leading and trailing edge in the RAM for that pixel.
- After receipt of the trailing edge, a sparse scan occurs independently in each column. Hit information is transferred to EOC buffers at column clock frequency.
- The common 22-bit data bus in the column pair as well as the EOC buffers are a single resource. Once hits are detected, left/right arbitration for permission to transmit occurs. The left hits are given priority over right hits.

## End of Column buffers:

- Each hit is assigned an EOC buffer using a sparse scan to locate the next free buffer (the buffer usage is not contiguous). For the 20 buffers in FE-B, this scan should easily complete in less than 25 ns.
- Each buffer includes 7-bits of LE in a CAM cell (write only store and compare cell), 7-bits of TE and 9-bits of address in an SRAM cell, and 4-bits of Trigger number in an second CAM cell. There are three basic state FF for Occupied, Triggered, and Readout states.
- Once the LE/TE/Address values for each hit are stored in an EOC buffer, the buffer is marked as Occupied. Each subsequent 40 MHz crossing then initiates a comparison between the LE timestamp in the buffer and the offset timestamp (displaced by L1 latency) which is produced by the timestamp generator block. If there is a timestamp match and no trigger accept is present, the Occupied flag is reset and the buffer location becomes free. If there is a L1 trigger coincidence, the Triggered flag is set, and the 4-bit Trigger Number is stored in a 4-bit CAM.
- The readout control logic in the chip periphery initiates event readout sequences whenever there are triggers pending in the Trigger FIFO. A 2D sparse scan is then performed over all of the EOC buffers, beginning with the top left (column 0). It is initiated by comparing the Trigger Number with the one for the current output event in the Trigger FIFO. All matching hits have their Readout flag set. The sparse scan then transfers hits sequentially using a 10 MHz clock.

## Overall logic:

- The timestamp generator block uses the 40 MHz clock to generate two 7-bit codes, one for the hit latching, and a second code displaced by the L1 latency for making trigger coincidences in the EOC buffers.
- The Trigger FIFO keeps track of up to 16 pending triggers (“events”) on the chip, recording the timestamp value and the overflow bit for each incoming L1 accept. The EOC buffers themselves record the trigger number (identical to the FIFO write pointer) for each hit which matches the timestamp of the trigger.
- The readout state machine then initiates a scan of the EOC buffers whenever there is a pending trigger in the FIFO. The FIFO read pointer provides the trigger number which is used to scan for all hits in the EOC belonging to this trigger. These hits are transferred from the EOC buffer block at 10 MHz and pushed through the subtractor and serializer blocks, and off of the chip.
- The TOT subtractor converts the LE/TE information to binary form and subtracts them to get the TOT in beam crossing units.
- The serializer transmits the data in the official 26 bit format (header bit, 4-bit trigger number, 8-bit row number, 5-bit column number, and 8-bit TOT value). The End-of-Event (EOE) word has the row number “F0” for normal data, and “E0” for data in which there is a buffer overflow warning flag set. If there are multiple hits in an event, or multiple events pending in the Trigger FIFO, the hit information is transmitted without gaps in the serial stream.

# Front-end Performance Measurements

## Threshold behavior:

- Threshold versus DAC settings (feedback, threshold adjustment DACs)
- Threshold versus input parameters (C(Load) and I(Leak))
- Threshold dispersion

## Noise behavior:

- Noise versus DAC settings (preamp bias, feedback, “shaping time”)
- Noise versus input parameters (C(Load) and I(Leak))

## Timewalk behavior:

- Timewalk versus DAC settings (preamp bias, diffamp bias, discriminator bias)
- Timewalk versus input parameters (C(Load) and I(Leak))

## TOT behavior:

- TOT response versus DAC settings (feedback
- TOT response versus input parameters (C(Load) and I(Leak))
- TOT dispersion

## Cross-coupling behavior:

- Measurements made for different detector types show values in the range of 1-3% depending on how much inter-pixel capacitance exists in the detector.

## Double-pulse resolution:

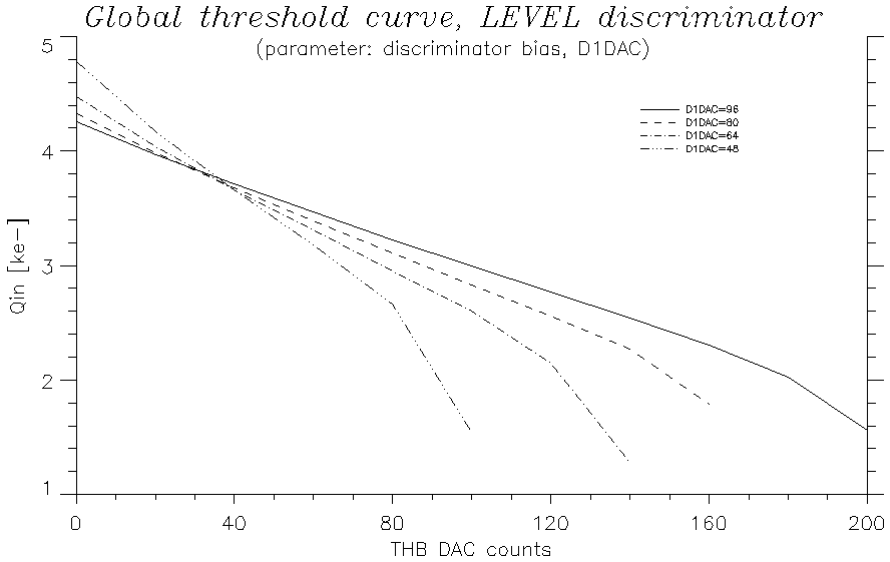
- Threshold shift as a function of input pulse amplitudes and separation

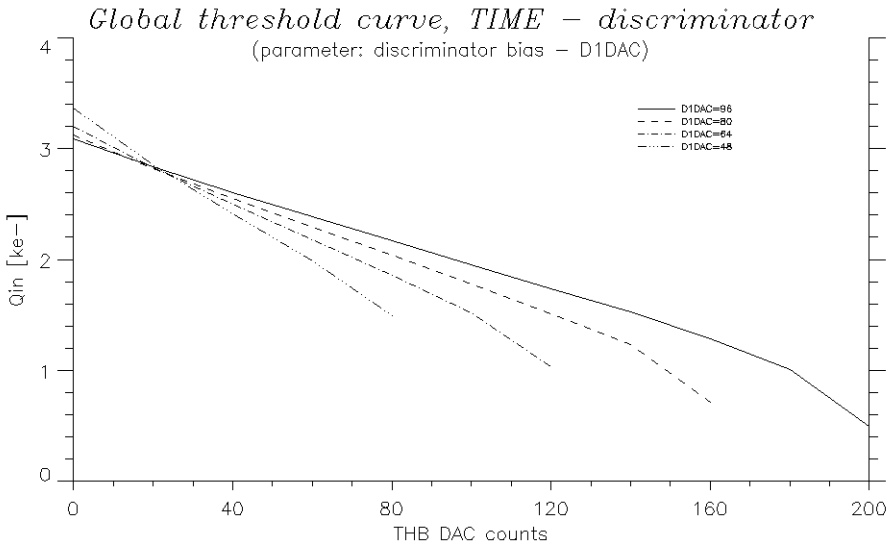
## Power Supply Rejection performance:

- Noise increase as a function of amplitude and frequency of power supply noise

# Threshold Behavior

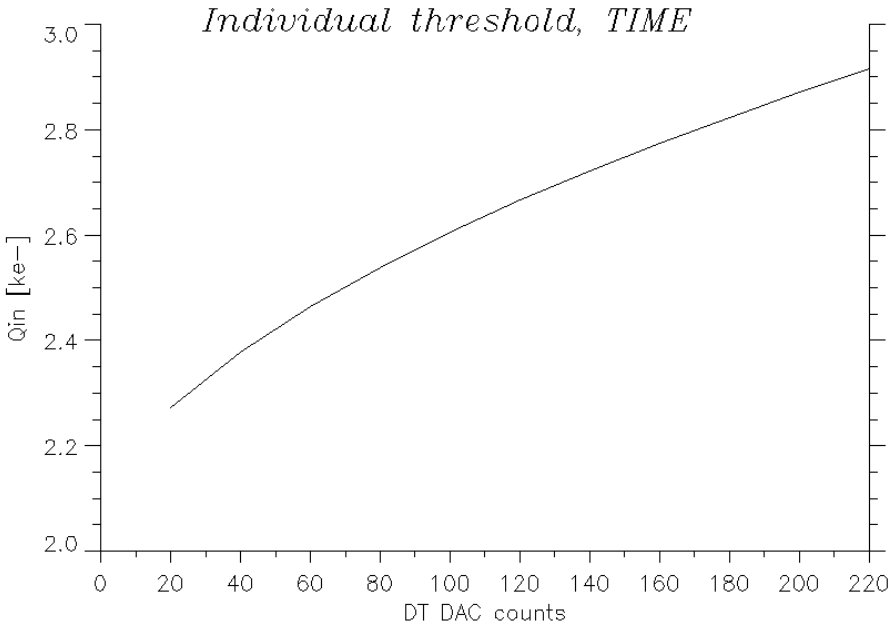
## Threshold as a function of the THBDAC settings:

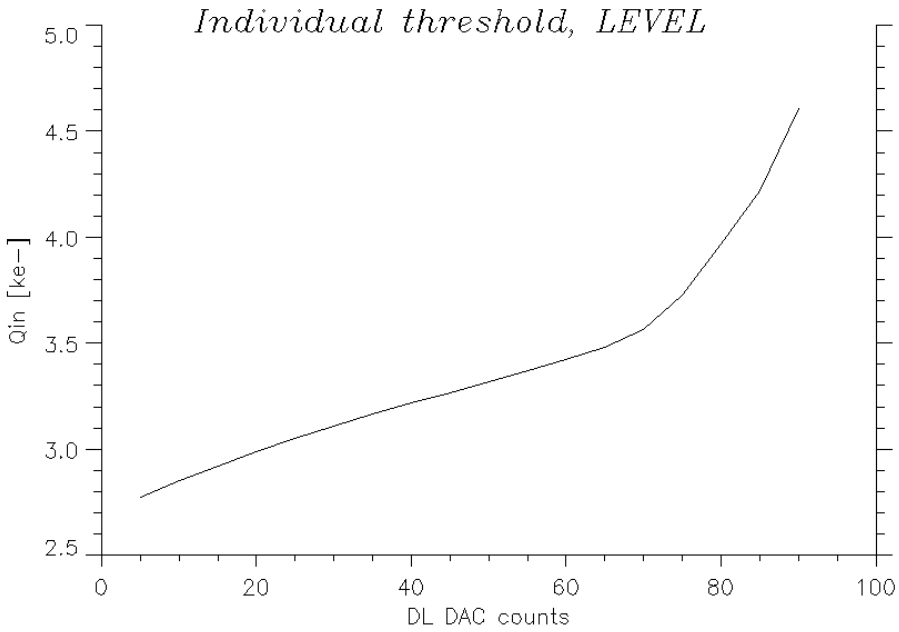



- THBDAC provides the global threshold adjustment.
- A value of 96 for D1DAC improves the timing performance of the front-end as well as providing a less sensitive adjustment of the threshold.

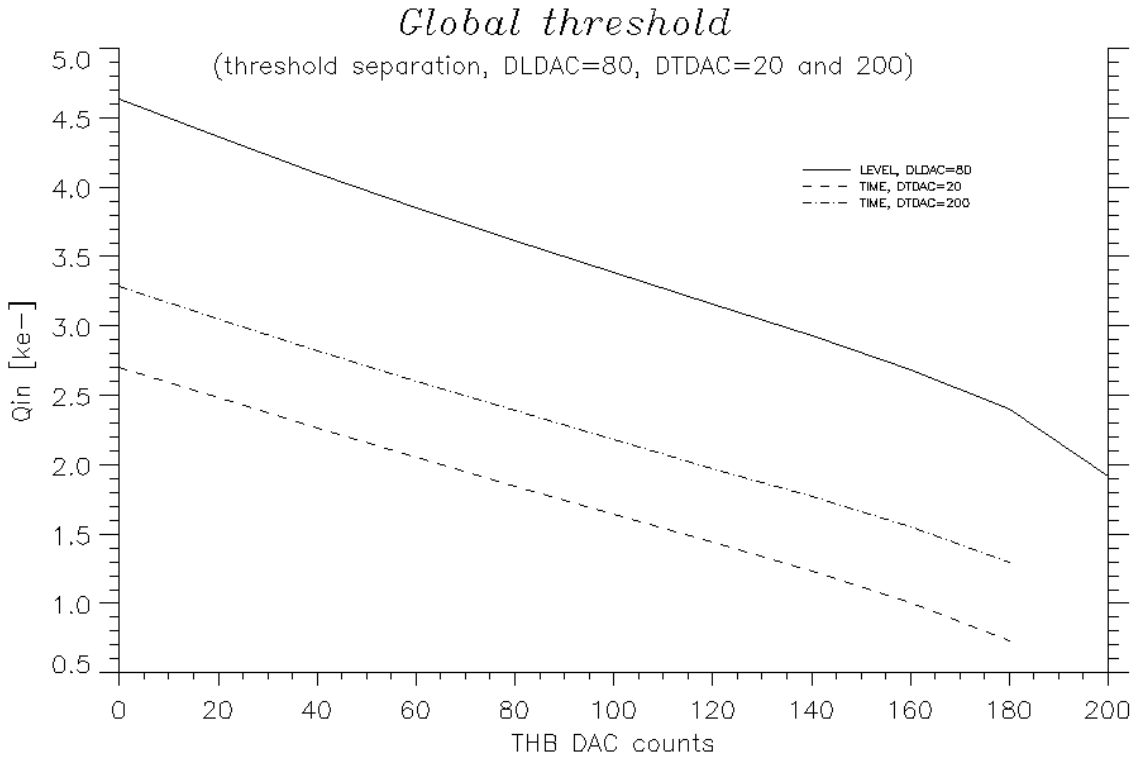
# Threshold as a function of the individual DAC settings:



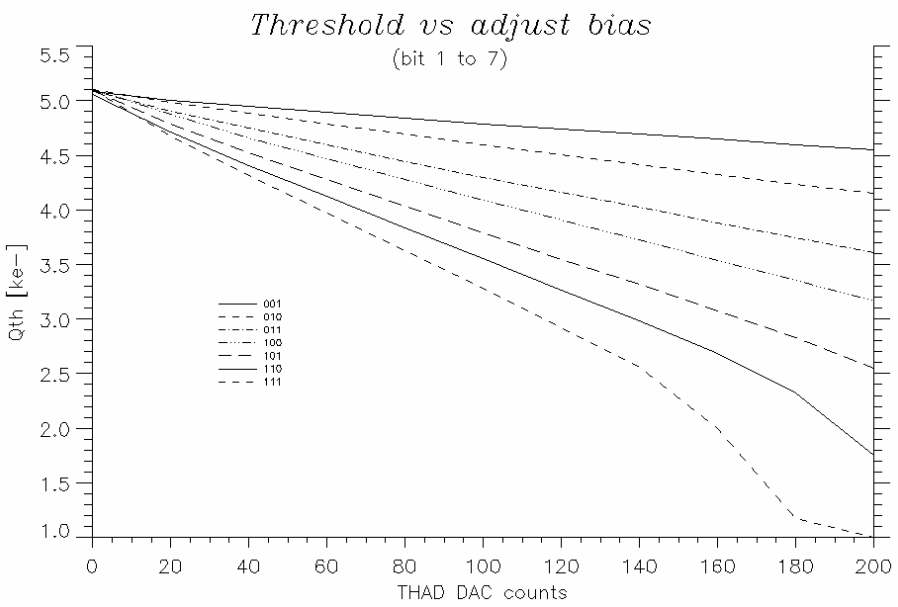

- Location of low (time) threshold can be fine-tuned with the bias. There is a modest effect on the timewalk performance, with higher biases giving slightly better performance.
- Location of high (level) threshold has a smaller range of adjustment.
- Adjustment of these two DACs is independent of the global THBDAC adjustment.
- In general, the separation adjustment is less flexible than we would have liked, and one of the reasons is that the diff-amp gain is slightly too high.

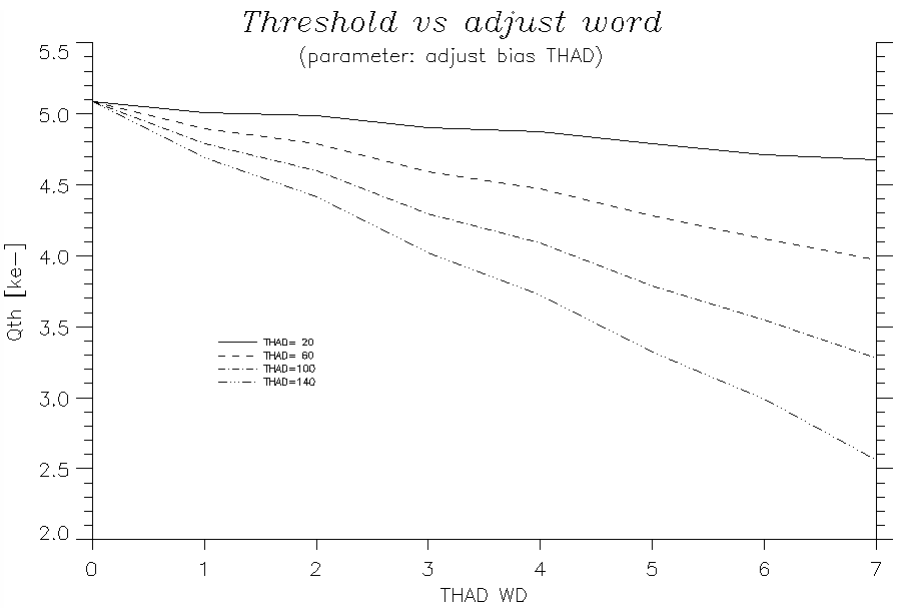
# Threshold separation as a function of DAC settings:




- Threshold separation is influenced somewhat by DTDAC, but the effect is not large. As far as the timewalk performance is concerned, the reduced threshold separation is partially compensated by the increased speed at higher DTDAC.

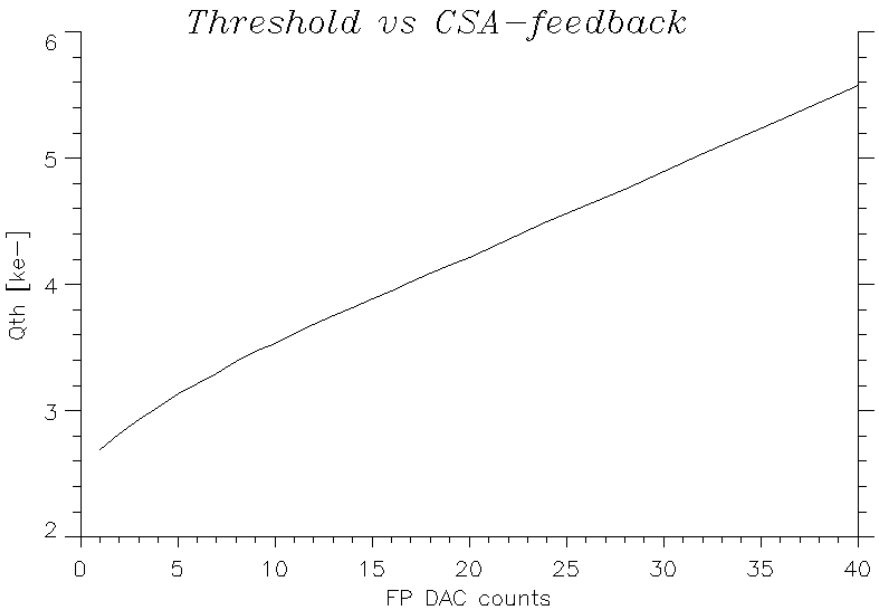
# Threshold adjustment using TDAC and THADAC:

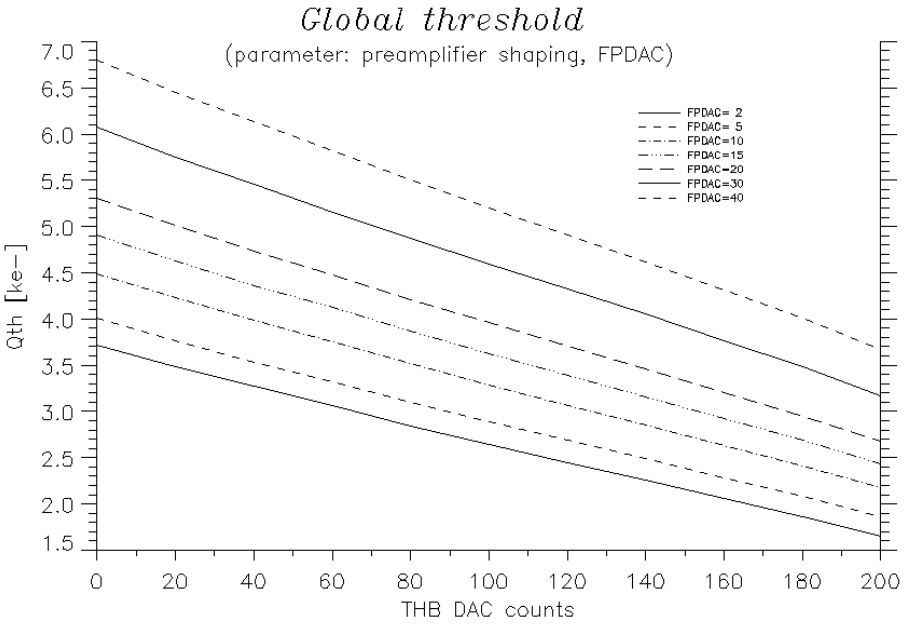



- For the 7 different values of TDAC setting, the threshold change with the step size (THADAC) behaves in a similar way to the adjustment using the THBDAC.
- Note that the values of TDAC which are loaded in the chip are the inverse of those shown here, so a value of 7 disconnects THADAC and gives the highest threshold, whereas a setting of 0 gives the lowest threshold.
- For a given THADAC setting, the 3-bit TDAC in the cell is also quite linear.

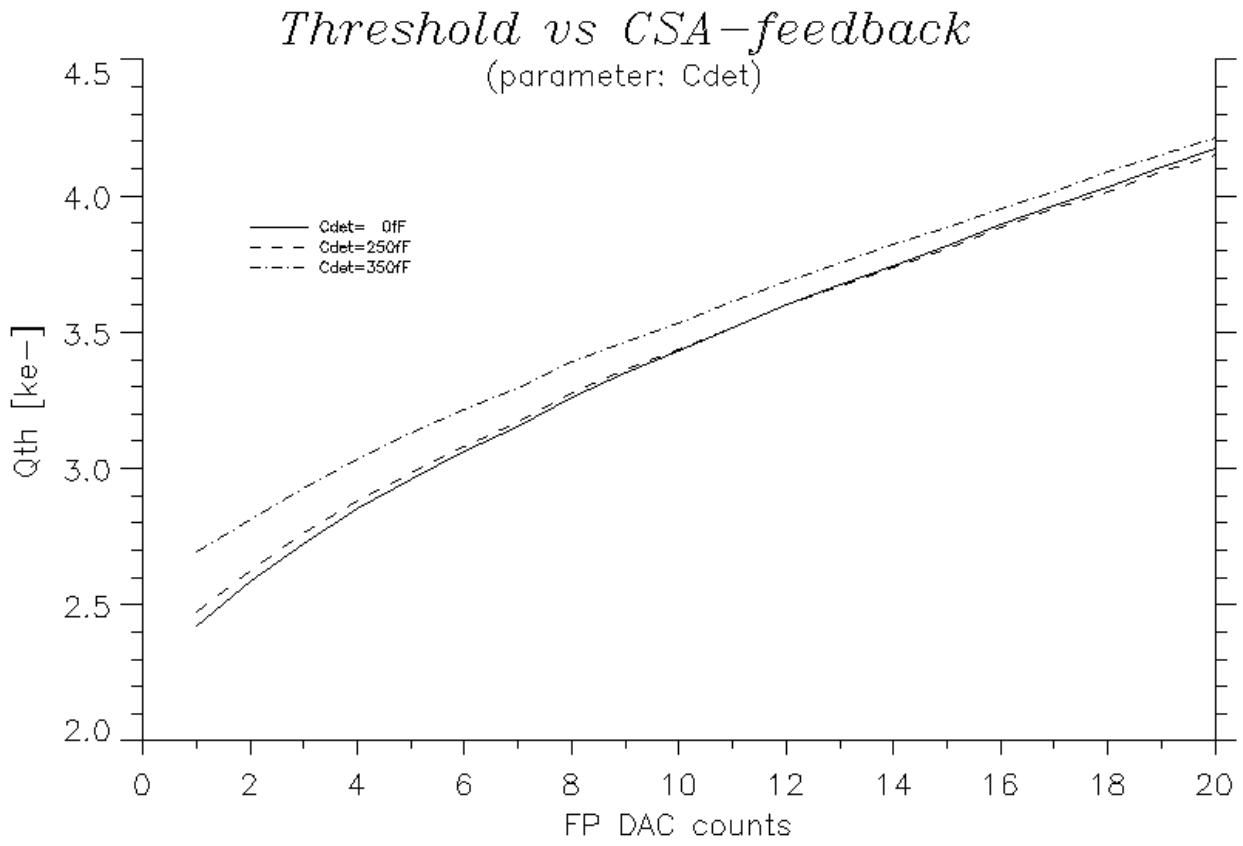
# Threshold as a function of the shaping time:



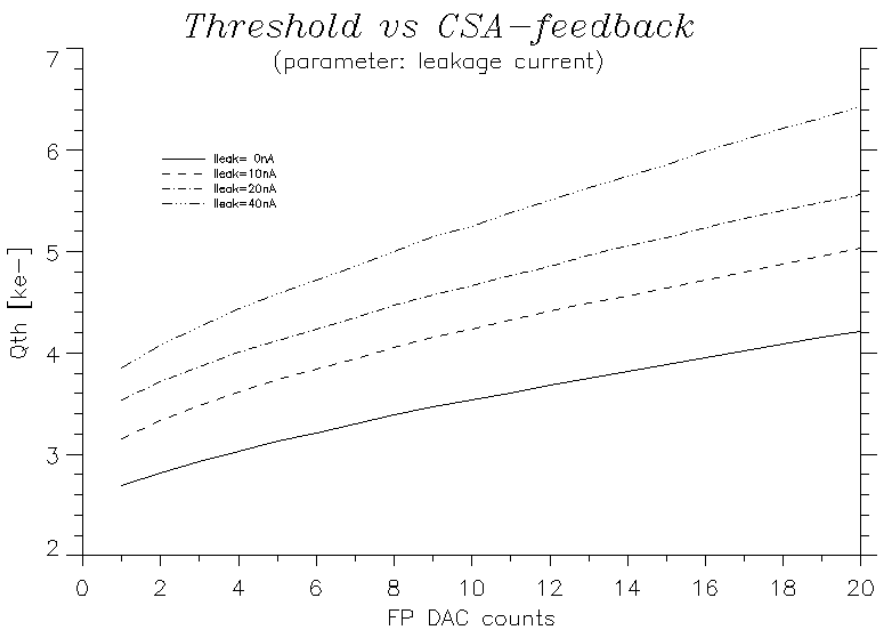

- Slower speed of diff-amp “integrates” over preamplifier pulse for time comparable to diff-amp risetime (about 70 ns in the current version). This makes the threshold sensitive to the shaping time (feedback current).
- FPDAC value of 20 is normal operating point for non-irradiated detectors (about 500 ns return to baseline for 20 Ke).

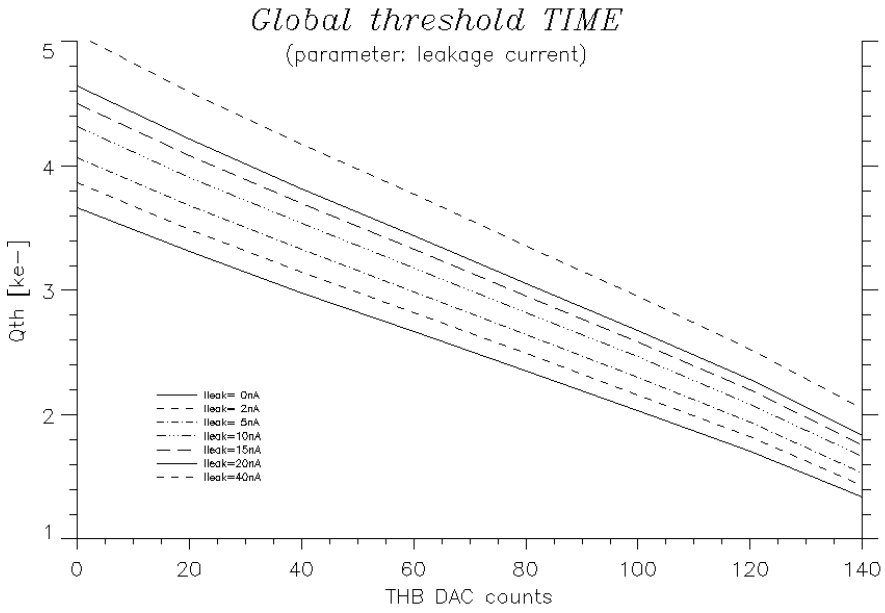
# Threshold as a function of C(Load):




- Very weak dependence of threshold on capacitive load. This is an indication that the preamplifier is doing its job properly - it has adequate gain-bandwidth...

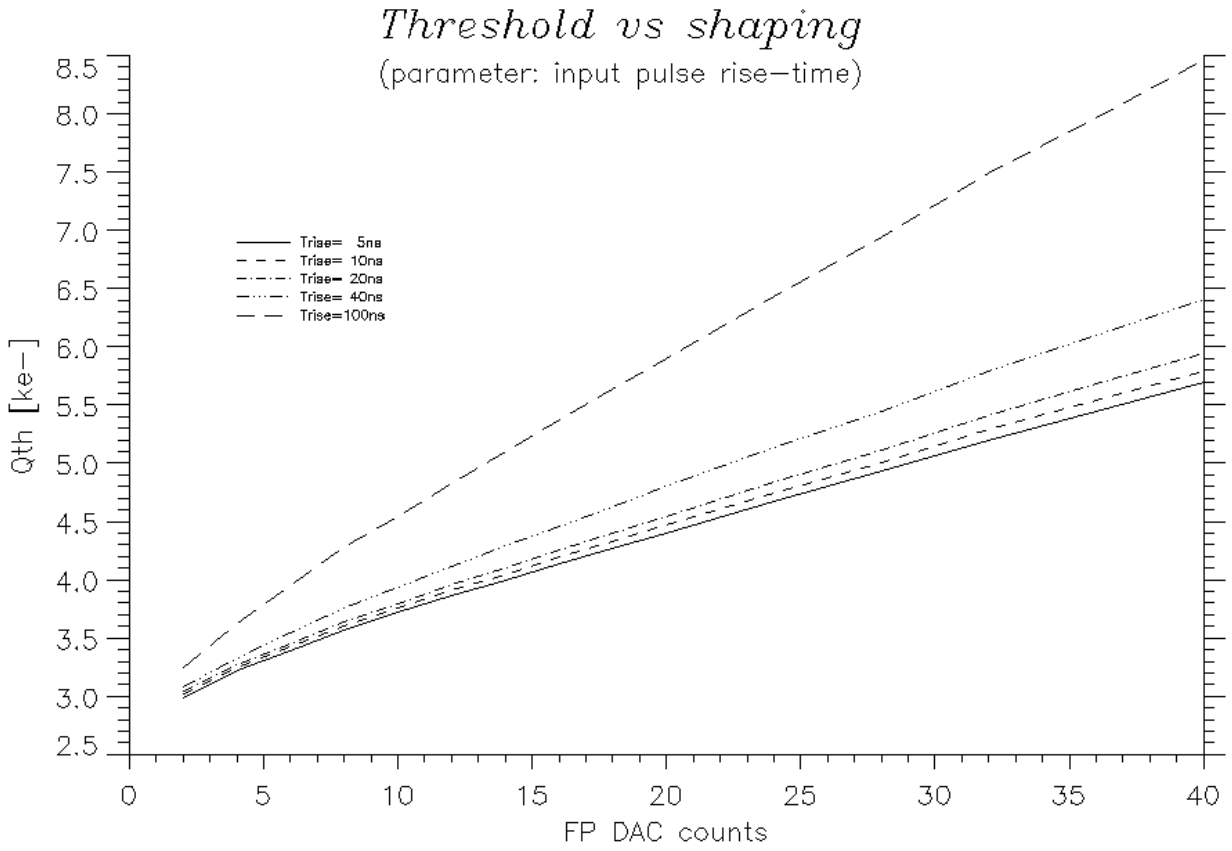
# Threshold as a function of I(leak):




- Variation with leakage current is significant. This is induced by the sensitivity of the threshold to the shaping time (shown already), which arises because of the speed of the diff-amp.
- With the CPPM feedback design, the shaping time is quite sensitive to the leakage current (see later TOT plots) - this is a probably an unavoidable side-effect of the leakage tolerance.
- The threshold shift with leakage is almost independent of the threshold itself.

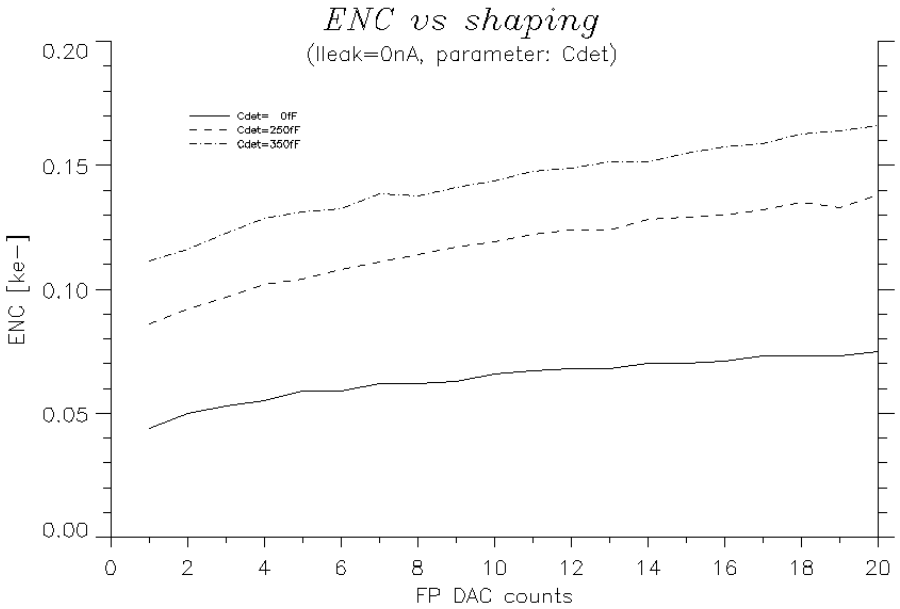
# Threshold as a function of input pulse risetime:

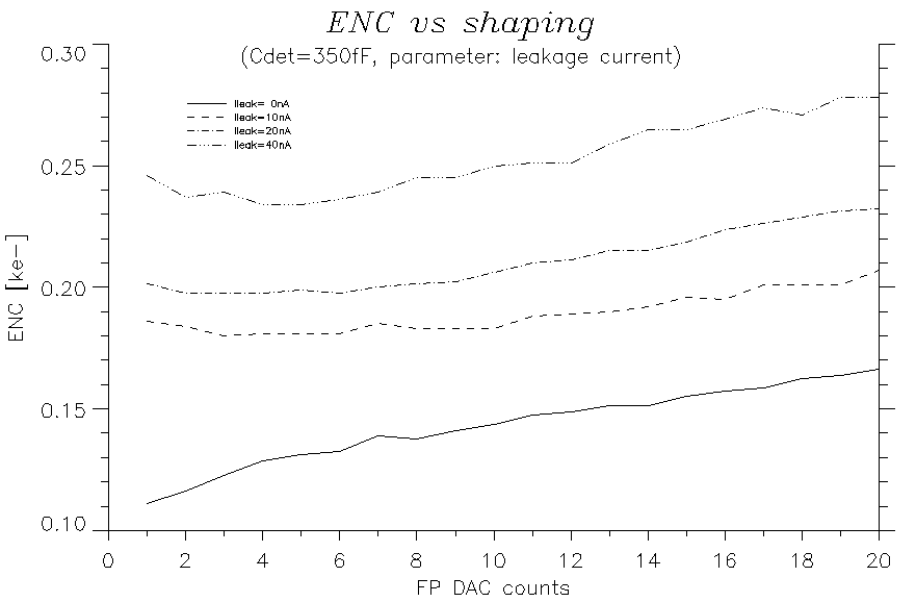



- Threshold (or effectively the preamplifier output pulse height) is sensitive to the risetime of the input pulse.
- For risetimes less than about 40 ns, there is little loss of input charge. Input signals need to be quite slow to fail to be registered...

# Noise Behavior

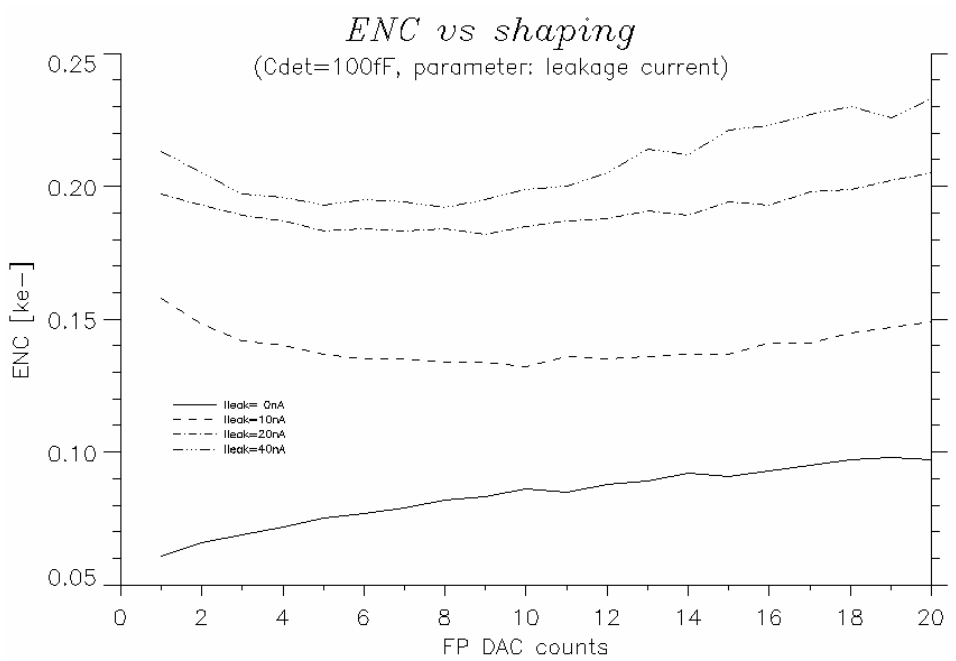
## Behavior of noise versus shaping, C(Load) and I(Leak):

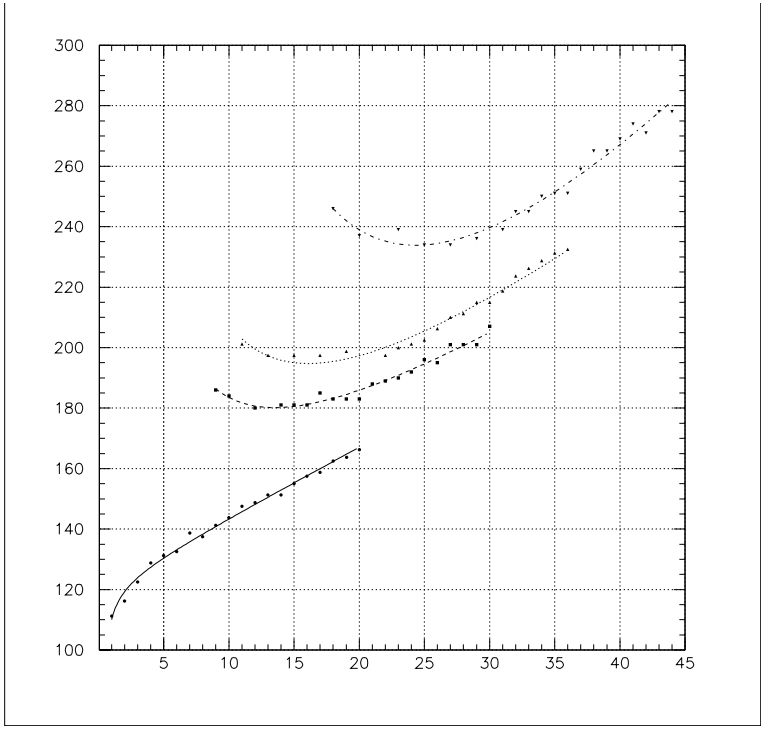



- With pure capacitive load, see expected trend in behavior of series noise as a function of shaping (triangular shaping of preamplifier is not easy to understand quantitatively). For FPDAC=20 to FPDAC=5, expect improvement of 140e to 100e for 250 fF C(Load).
- Addition of leakage current (parallel noise source) increases the noise, and creates an “optimal” shaping time. The result is also to flatten the noise behavior as a function of the shaping time. For 20 nA, FPDAC=20 to FPDAC=5, expect improvement of 230e to 200e for 350fF C(Load).

- Note that for a given FPDAC setting, the shaping time decreases with leakage current, so the rise in noise is partly an increase in the serial noise from increased shaping, and partly the contribution from the parallel noise itself.

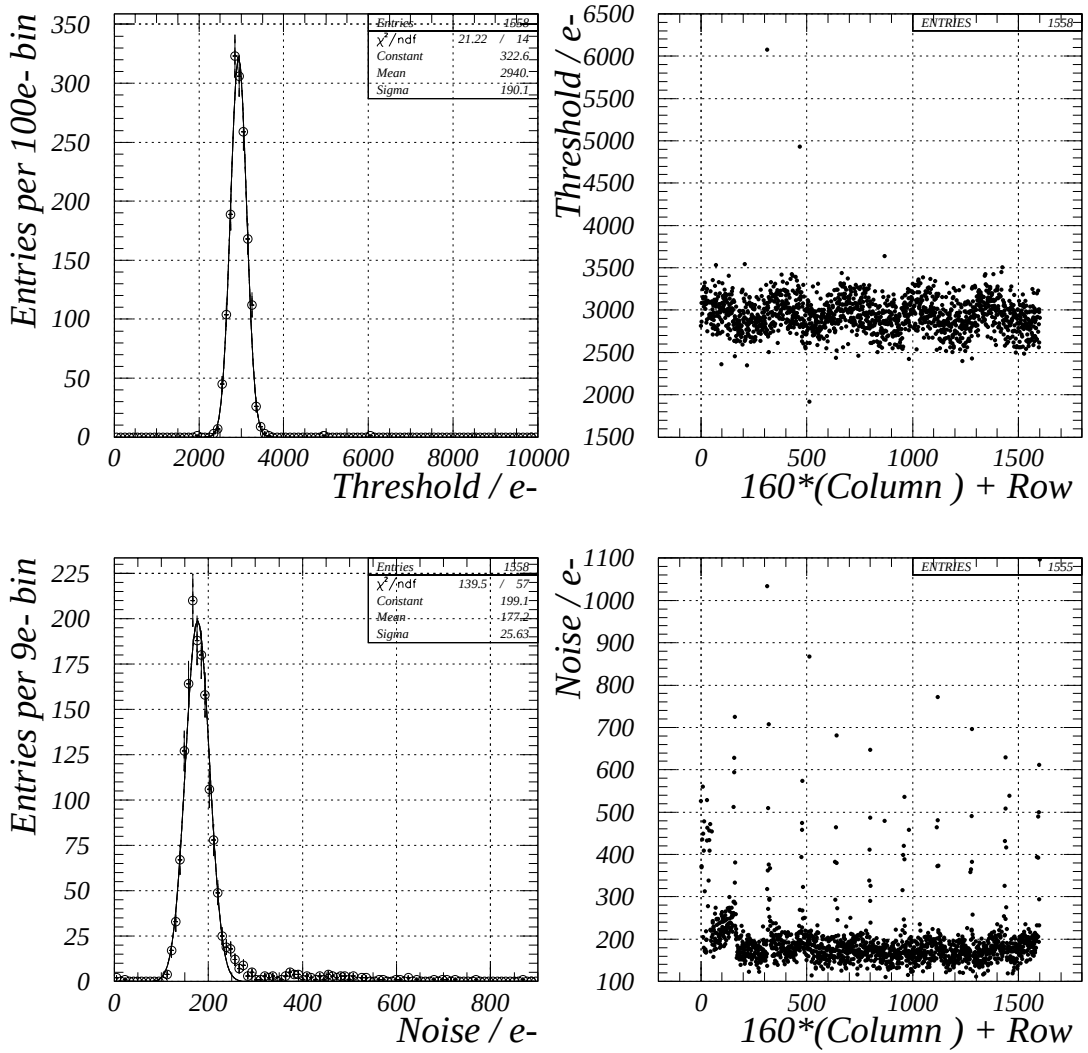


- Plot on the right rescales the shaping times for different leakage currents, so that a given vertical slice through all of the curves represents a constant shaping time. Longer shaping times are on the left. The curves correspond to 0, 10, 20, and 40 nA of leakage current. This demonstrates that until a large leakage value of 40 nA is reached, much of the noise increase in the plots on the left arises from increased series noise due to the shaping changes.

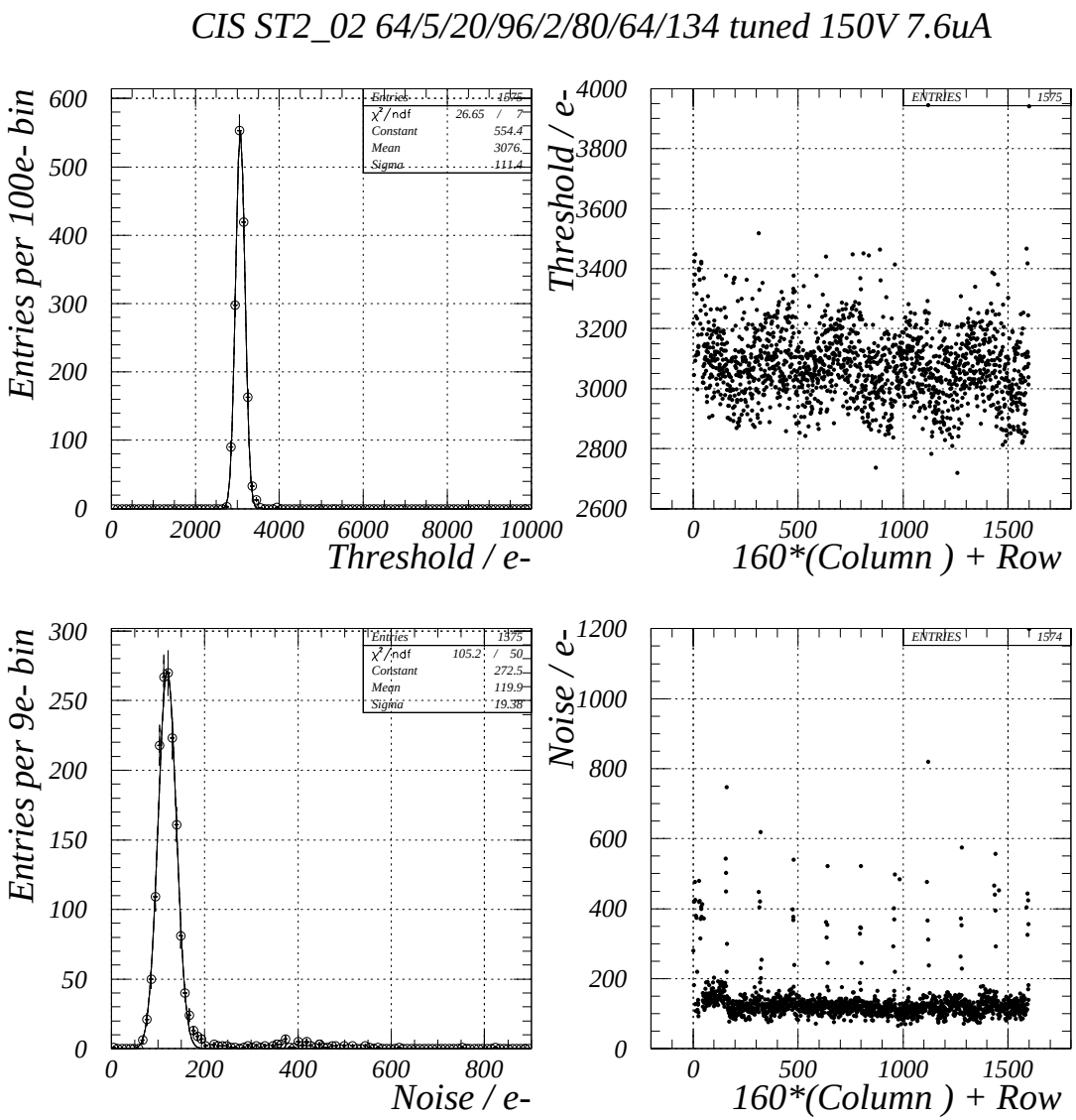
# Threshold dispersion and noise dependence on shaping:

*CIS ST2_02 64/20/20/96/96/80/64/134 tuned 150V 7.6uA*



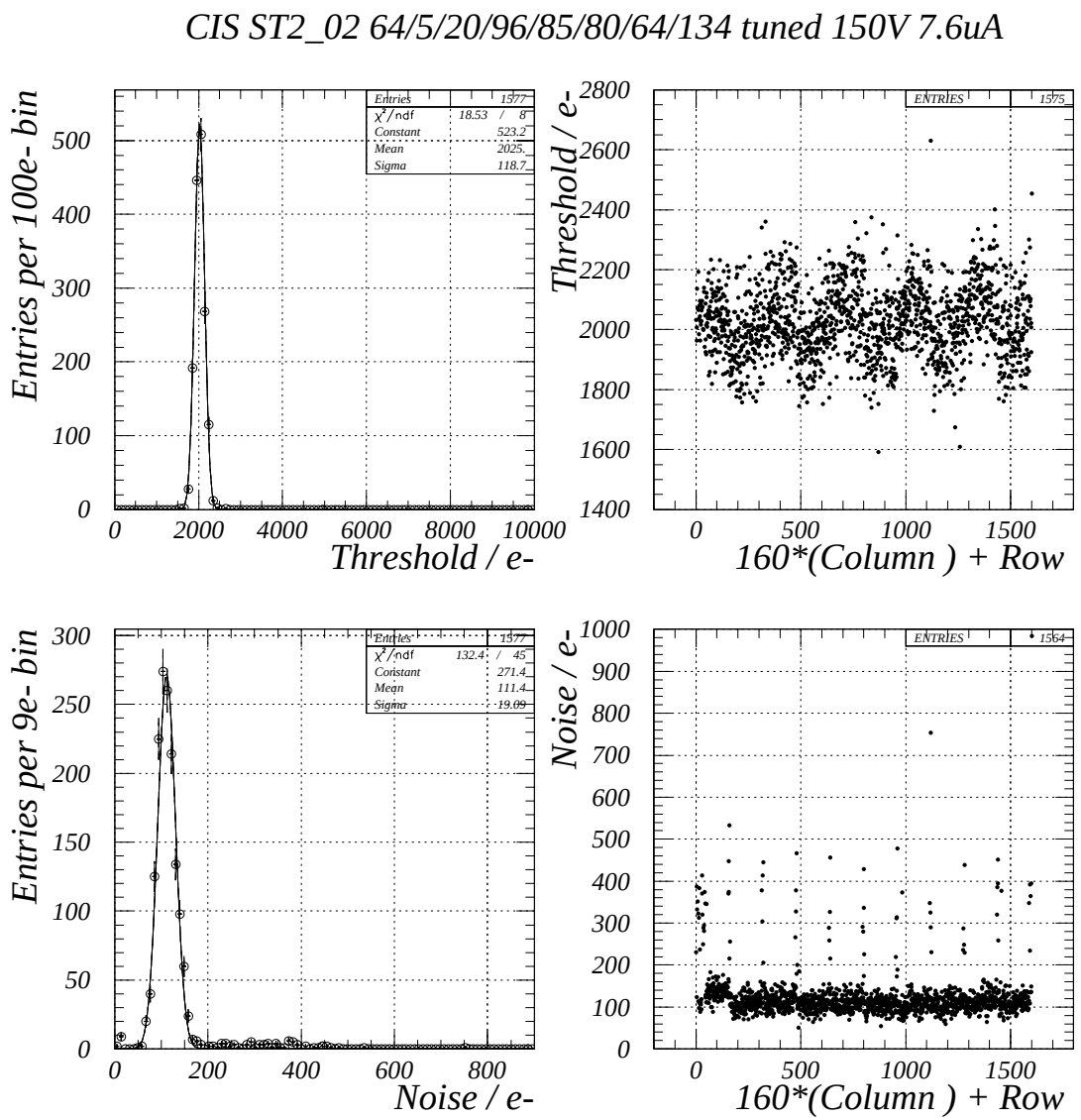

- Threshold scan for standard operating conditions (FPDAC=20).
- Threshold dispersion of an ST2 detector after threshold tuning. Attempt to capture all channels in distribution, sigma = 190e.
- Average noise is about 180e.

# Threshold dispersion and noise with increased shaping:




- Threshold scan with reduced feedback current (FPDAC=5).
- Dispersion is reduced from 190e to 110e
- Noise is reduced from 180e to 120e.

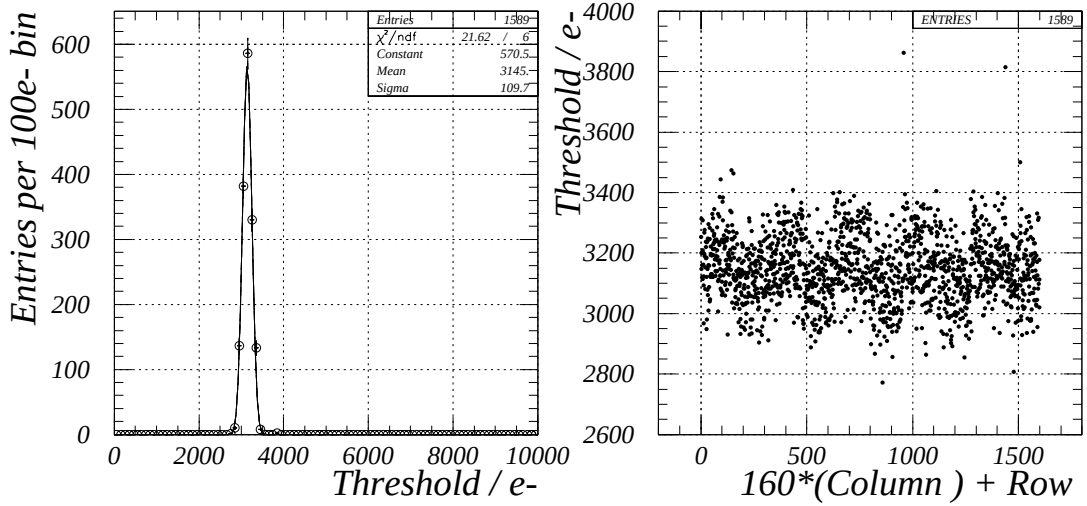
# Threshold dispersion and noise with reduced threshold:

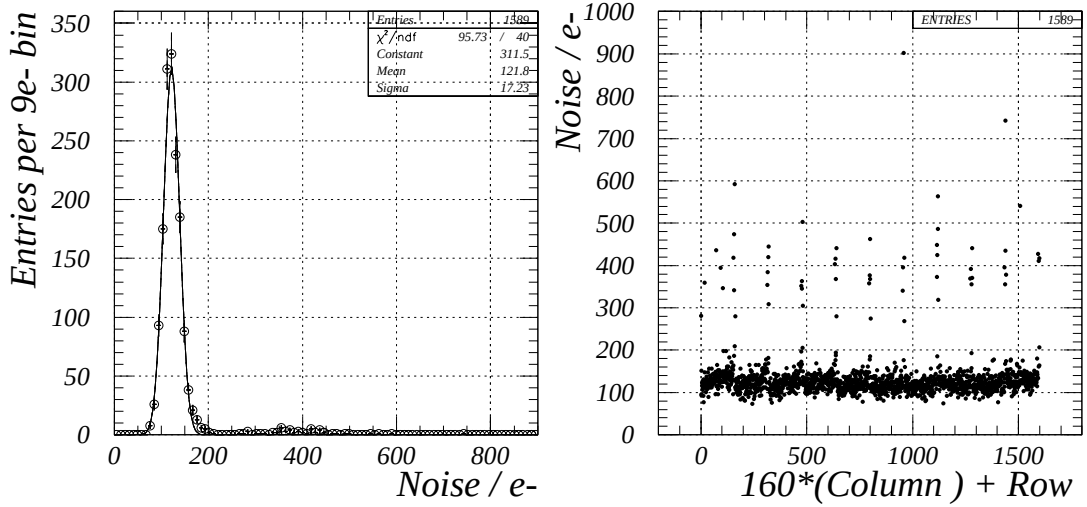



- With the reduced noise and threshold dispersion, operation at lower thresholds becomes possible (below 2Ke for the high threshold, and hence about 1Ke for the low threshold).
- Threshold dispersion is unchanged at 120e.
- The average noise is also unchanged at 110e.

# Threshold dispersion and noise for ST1 Detector:

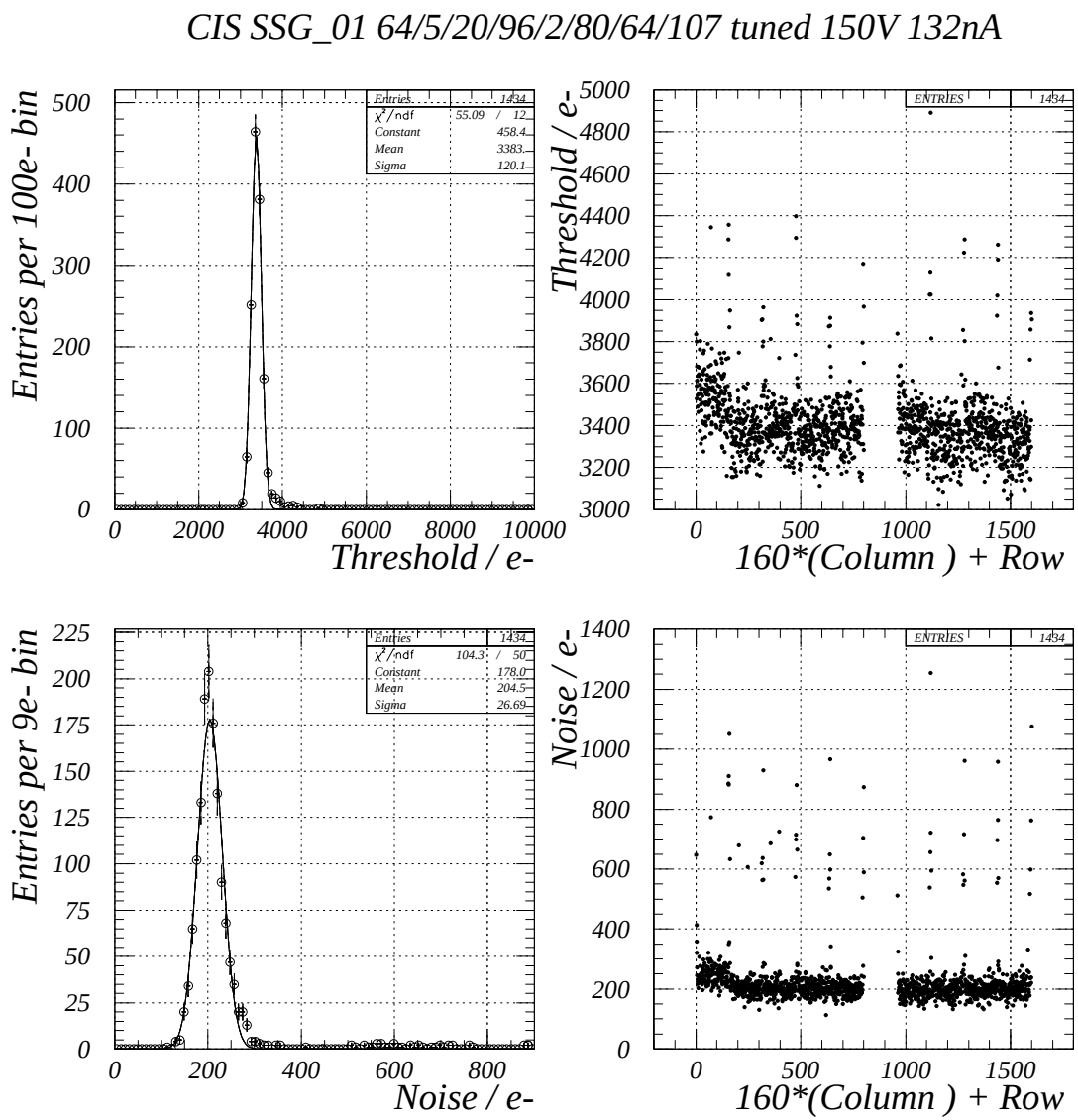
*CIS ST1_01 64/5/20/96/28/80/64/107 tuned 150V 21nA*




- The performance of this detector is similar to ST2 for FPDAC=5.
- The threshold dispersion is only 110e
- The average noise is about 120e.

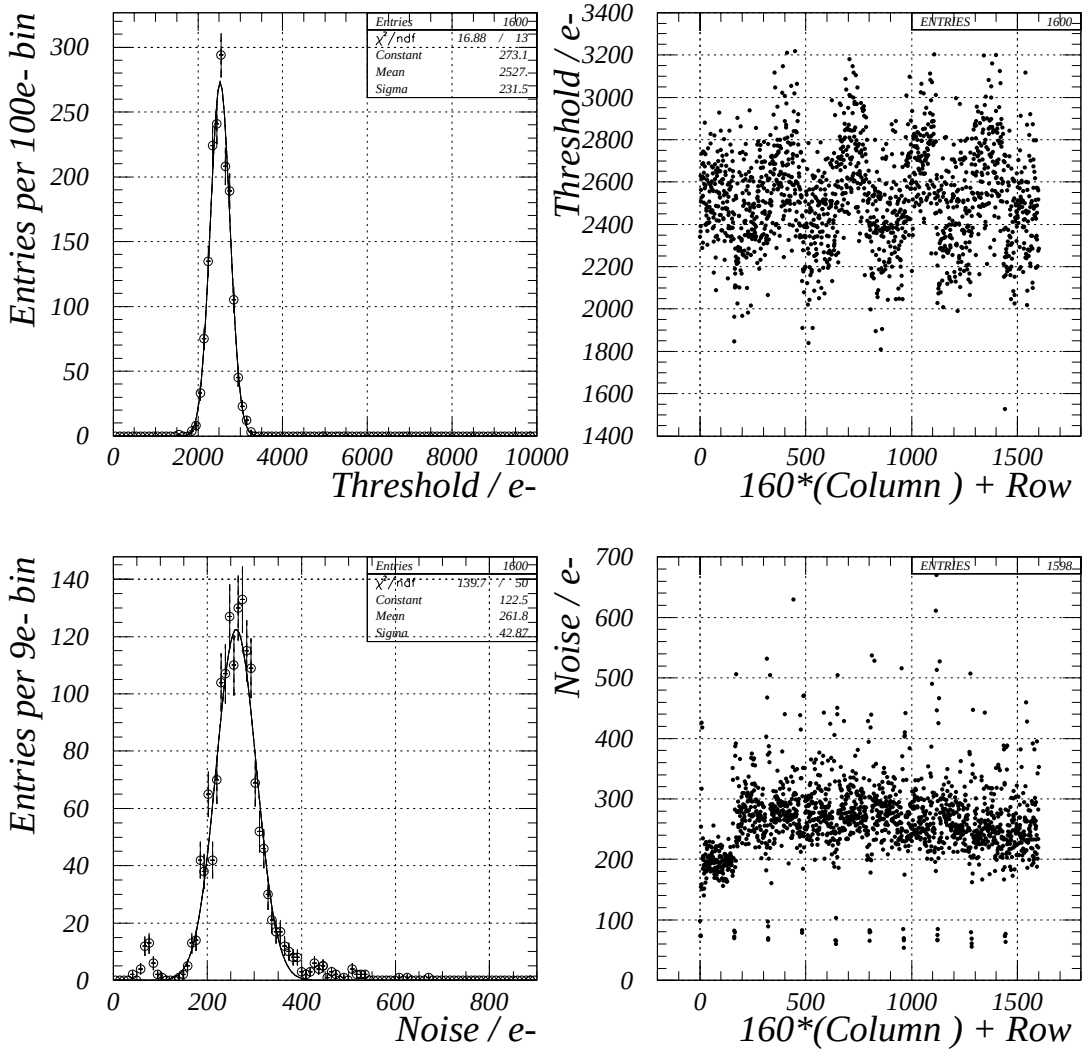
# Threshold dispersion and noise for SSG Detector:




- This detector has a significantly larger inter-pixel capacitance.
- Threshold dispersion is still small, about 120e
- Average noise is increased to about 205e.
- One column of this device apparently died during testbeam operation - the only known casualty so far.

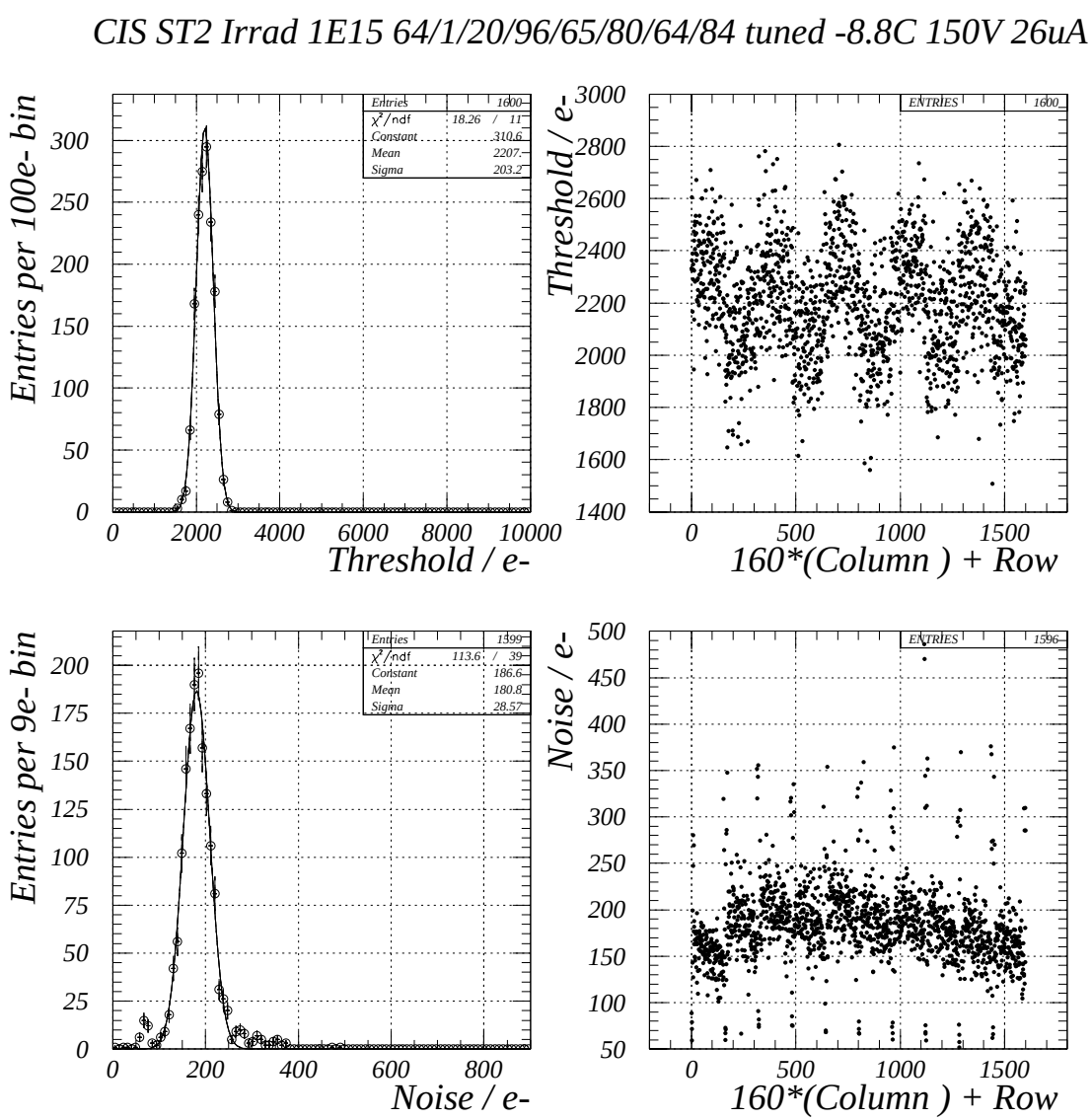
# Threshold dispersion and noise with leakage current:

*CIS ST2 Irrad 1E15 64/1/20/96/65/80/64/84 tuned -8.8C 600V 63uA*




- Threshold scan for irradiated detector, operating with about 60 µA bias, or about 20 nA/ pixel, at 600V.
- This ST2 detector was exposed to $10^{15}$ equivalent flunce.
- Threshold dispersion is 230e. Average noise is 260e. Test chip predicts noise of about 200e.
- Note: with 20 nA/pixel leakage, even FPDAC=1 gives a fairly short shaping time (about 1µs).
- Low noise pixels are not connected in double metal design.

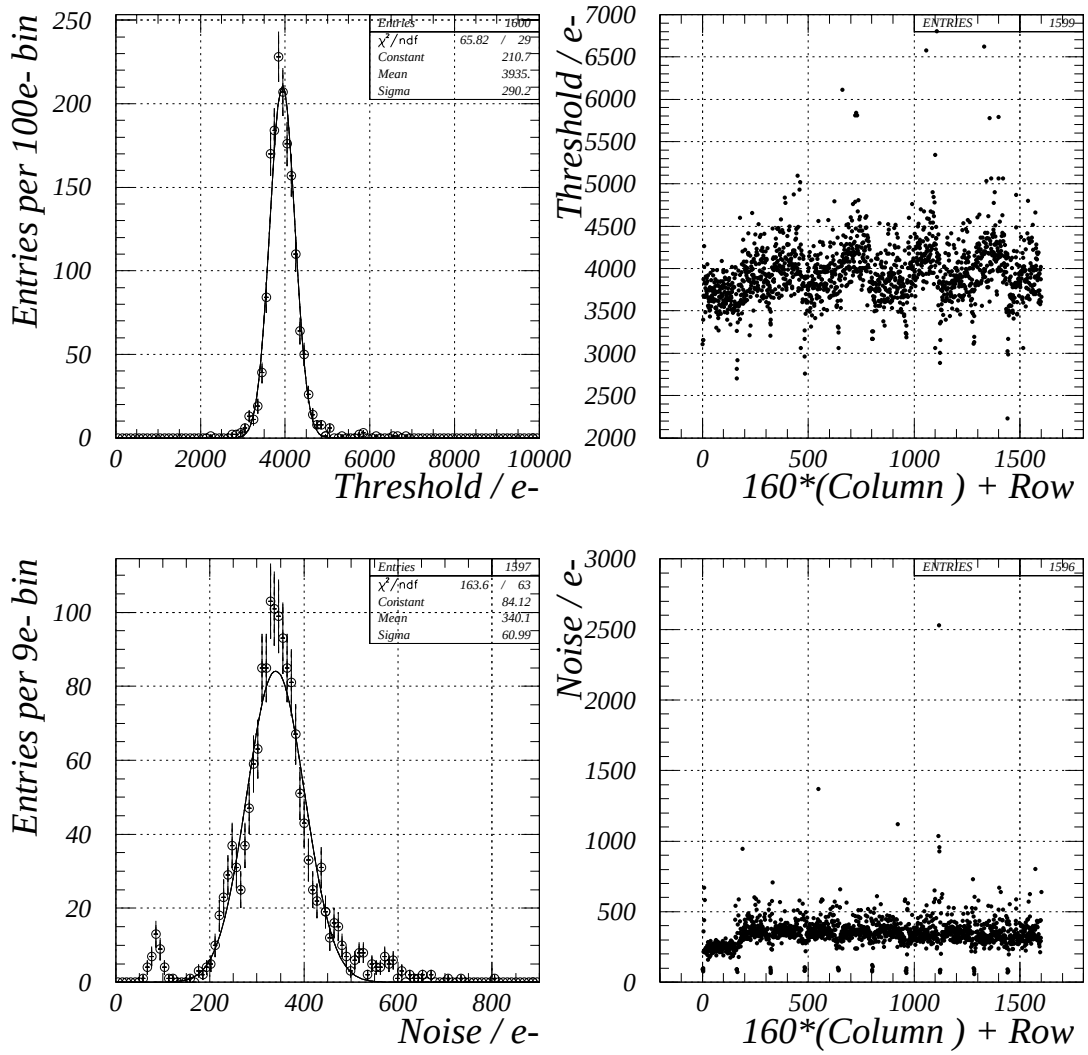
# Threshold dispersion and noise with smaller leakage:




- Performance of same irradiated detector with 150V bias, 26 µA of leakage, or about 10 nA/pixel.
- Threshold dispersion is 200e.
- Average noise is 180e.

# Threshold dispersion and noise with large leakage:

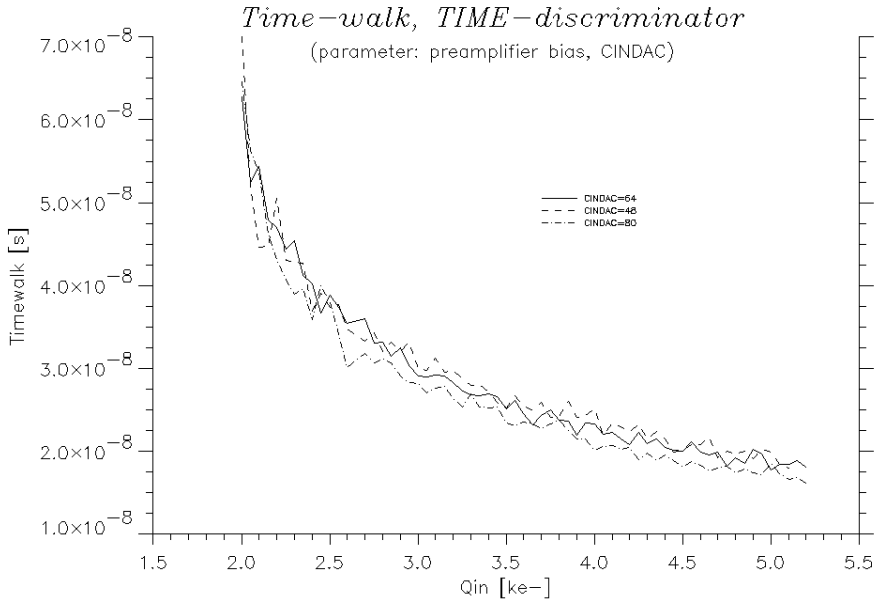
*CIS ST2 Irrad 1E15 64/1/20/96/2/80/64/84 tuned -1.5C 500V 153uA*

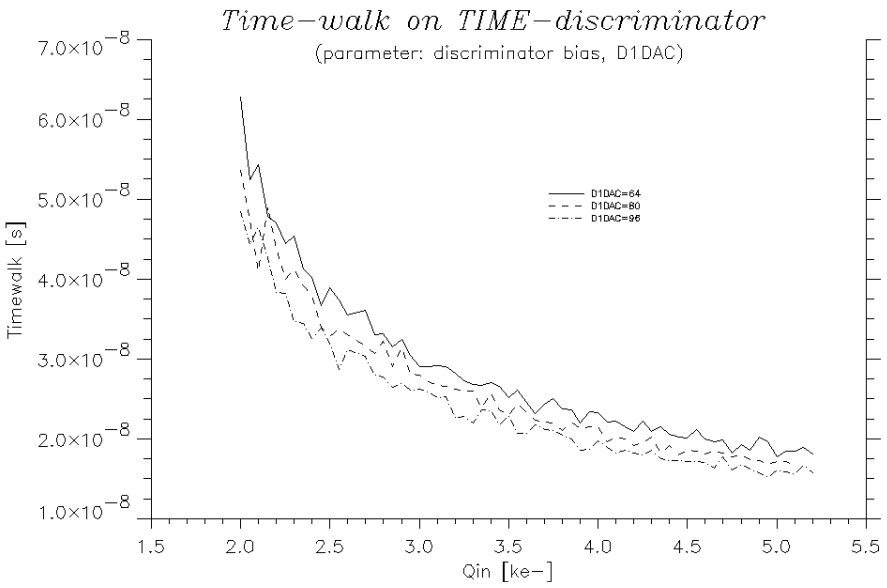



- Threshold scan of same irradiated detector with 153 μA, or about 50 nA/ pixel leakage. The voltage is still 600V, but the temperature was increased to roughly double te leakage.
- Threshold dispersion is 290e (about same)
- Average noise is 340e. Expect a value of about 250e for this shaping and this leakage based on test chip measurements.

# Timewalk Behavior

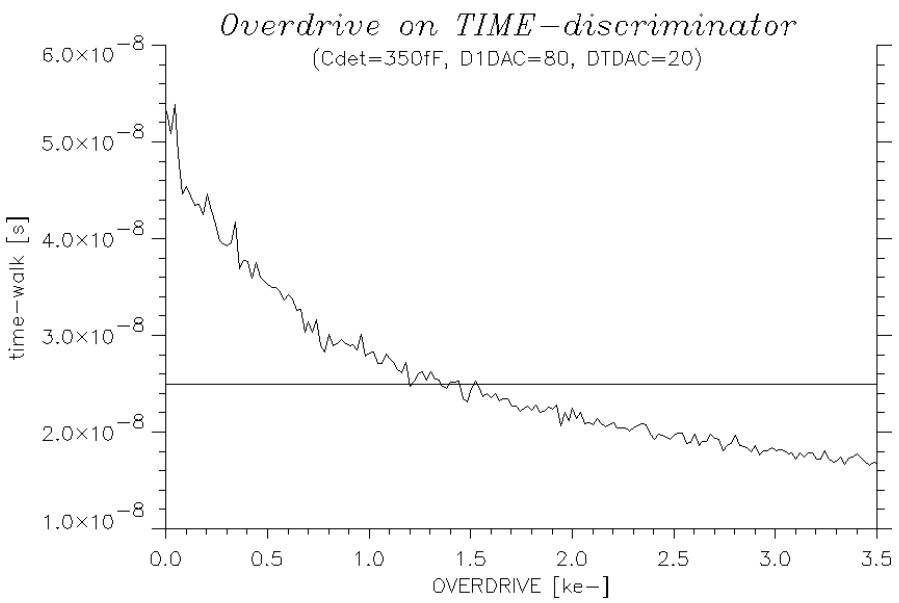
## Behavior of timewalk (without C(Load)) vs DACs:

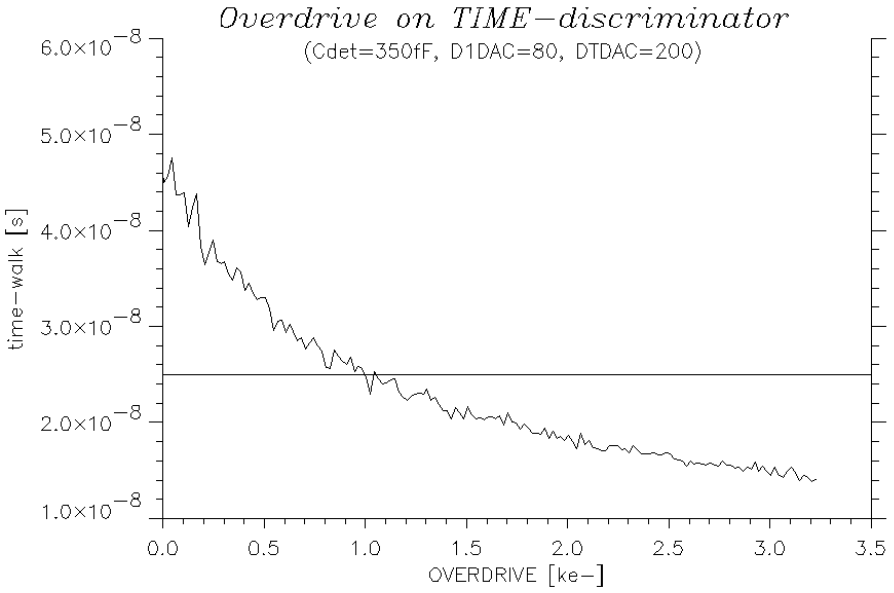



- Vary both CINDAC (preamp bias) and D1DAC (diff-amp bias).
- Varying preamp bias has little effect on timewalk performance
- Varying diff-amp bias should improve speed and give reduced timewalk. A modest effect is in fact seen...

# Behavior of timewalk with C(Load):

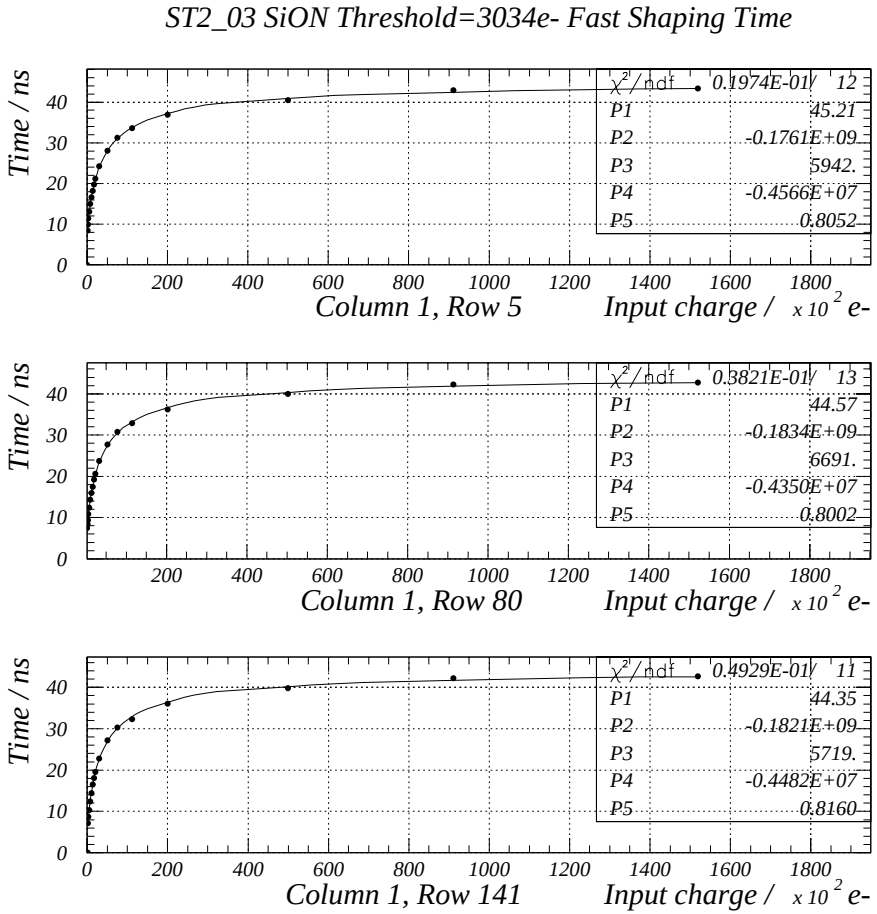



- Required overdrive of low threshold (time) discriminator depends on bias.
- The lower DTDAC gives slightly worse timewalk performance for this discriminator alone.
- The large DTDAC value gives a smaller discriminator separation, and so changes the charge value for which out-of-time hits are suppressed.

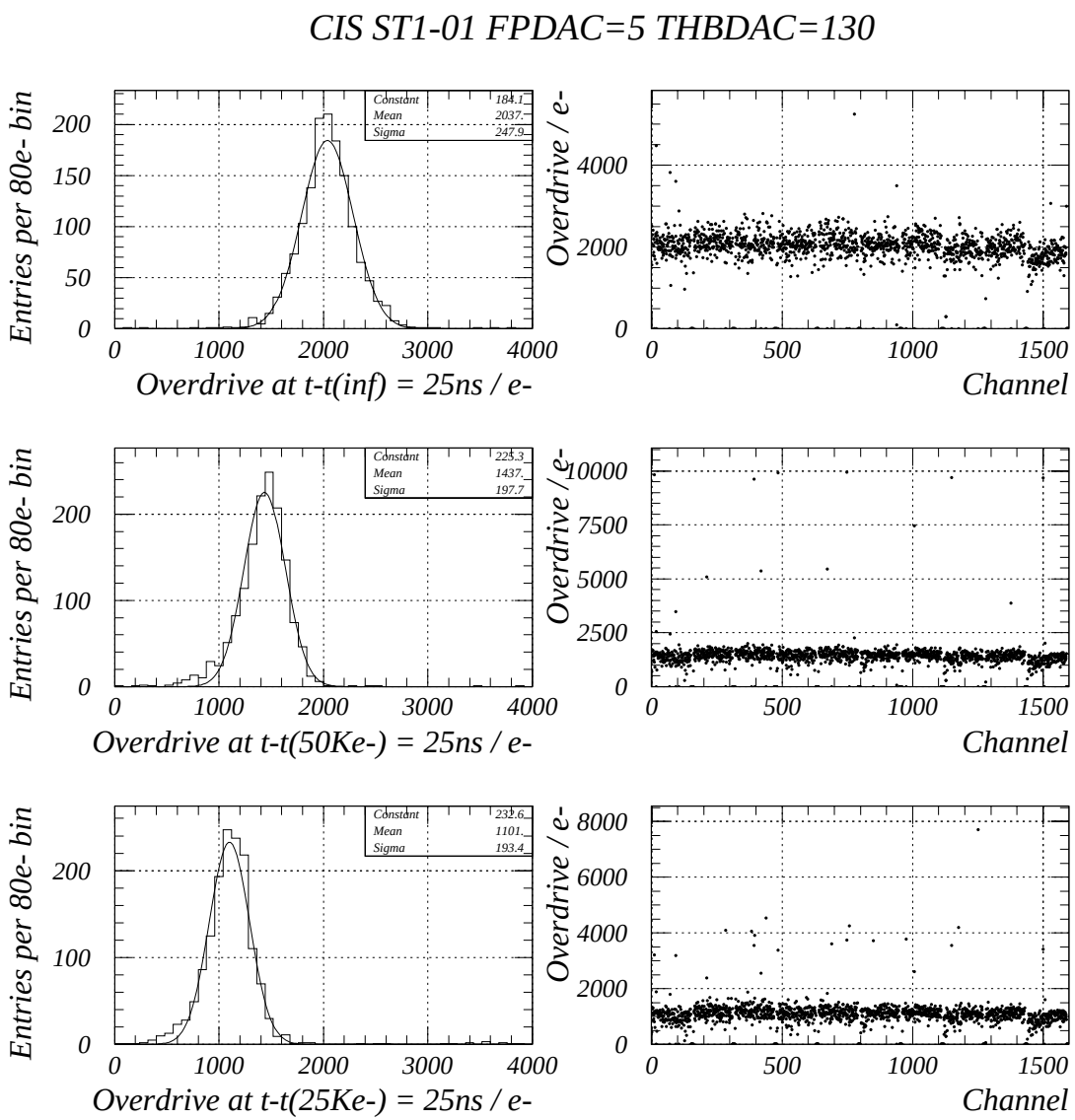
# Measurement of timewalk in the full FE-B array:

- Use strobe delay on PCC to step time in 0.25ns units (256 steps), and step charge in 18 non-uniform steps. For each charge, the timing is measured by looking for the time at which a hit moves form one BCO to the next.
- The resulting data points are fit with a polynomial to allow interpolation or extrapolation to find the timewalk for any given charge:



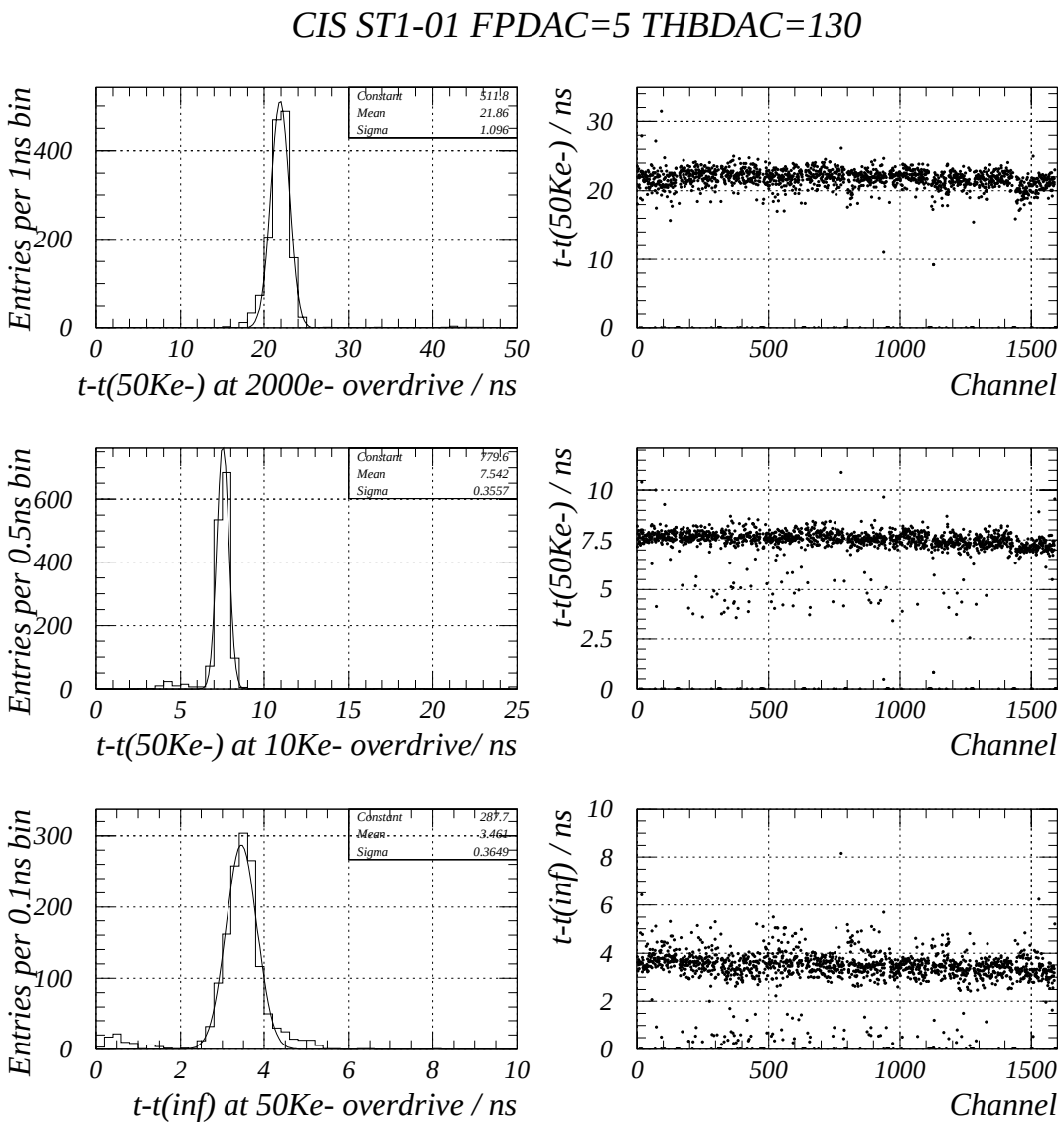

- These measurements were made using the internal chopper circuit in FE-B in order to inject the required large charges. The thresholds were cross-calibrated against an external LeCroy pulser, and the internal scan typically produced a 1.1Ke offset relative to the precise external calibration.
- Scans using both choppers were systematically compared, and after correction for the offset, no further differences were observed.

# Timewalk scan for ST1 detector at 2.2Ke threshold:



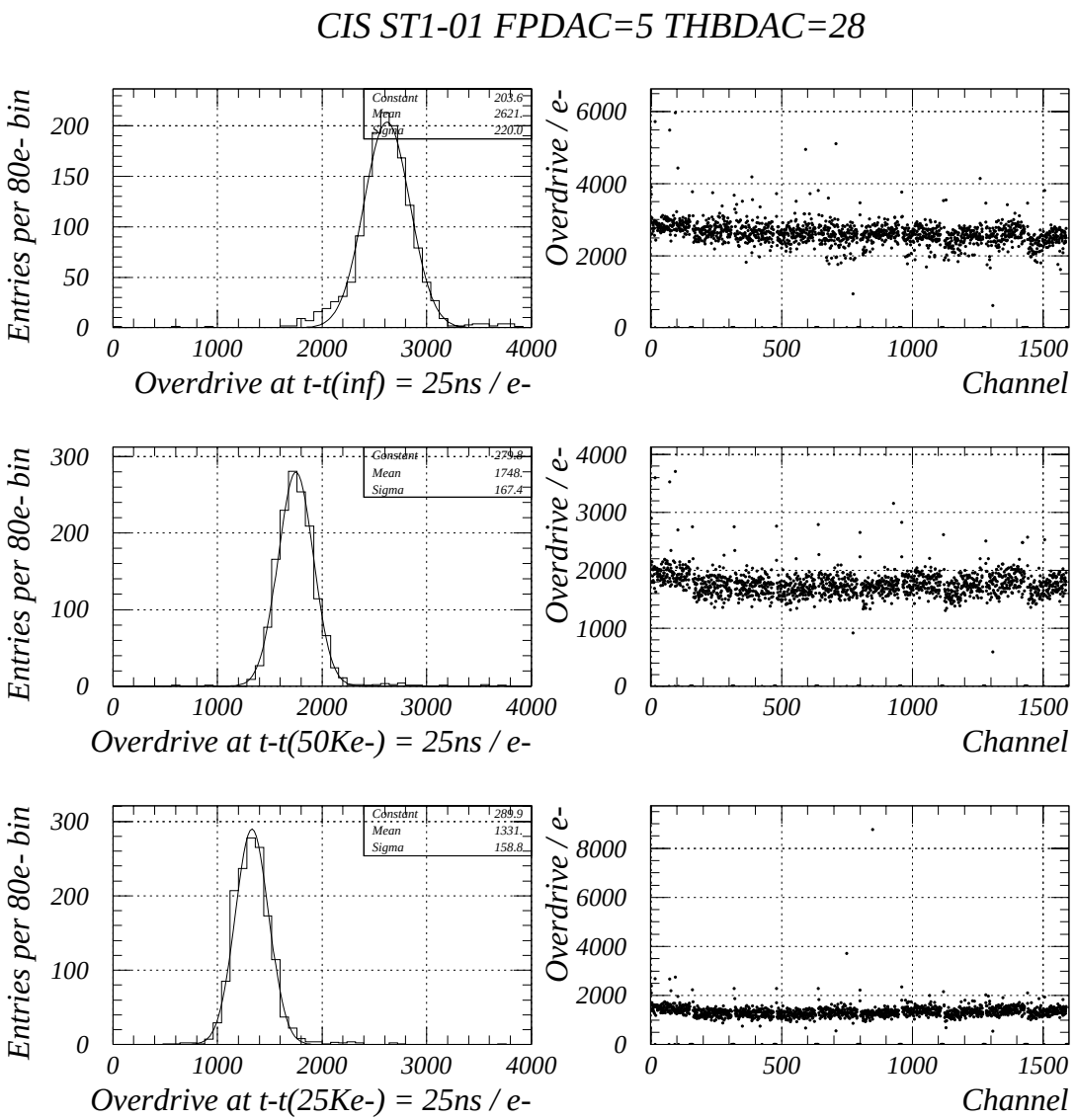

- Calculate overdrive by extrapolating to reference time for 50Ke charge, finding the input charge corresponding to 25 ns of timewalk, and then subtracting the fitted threshold for that pixel.
- At this low threshold, with this long shaping time (FPDAC=5), the required overdrive is about 1.4Ke above the high threshold.

# Detailed timing information for the previous scan:



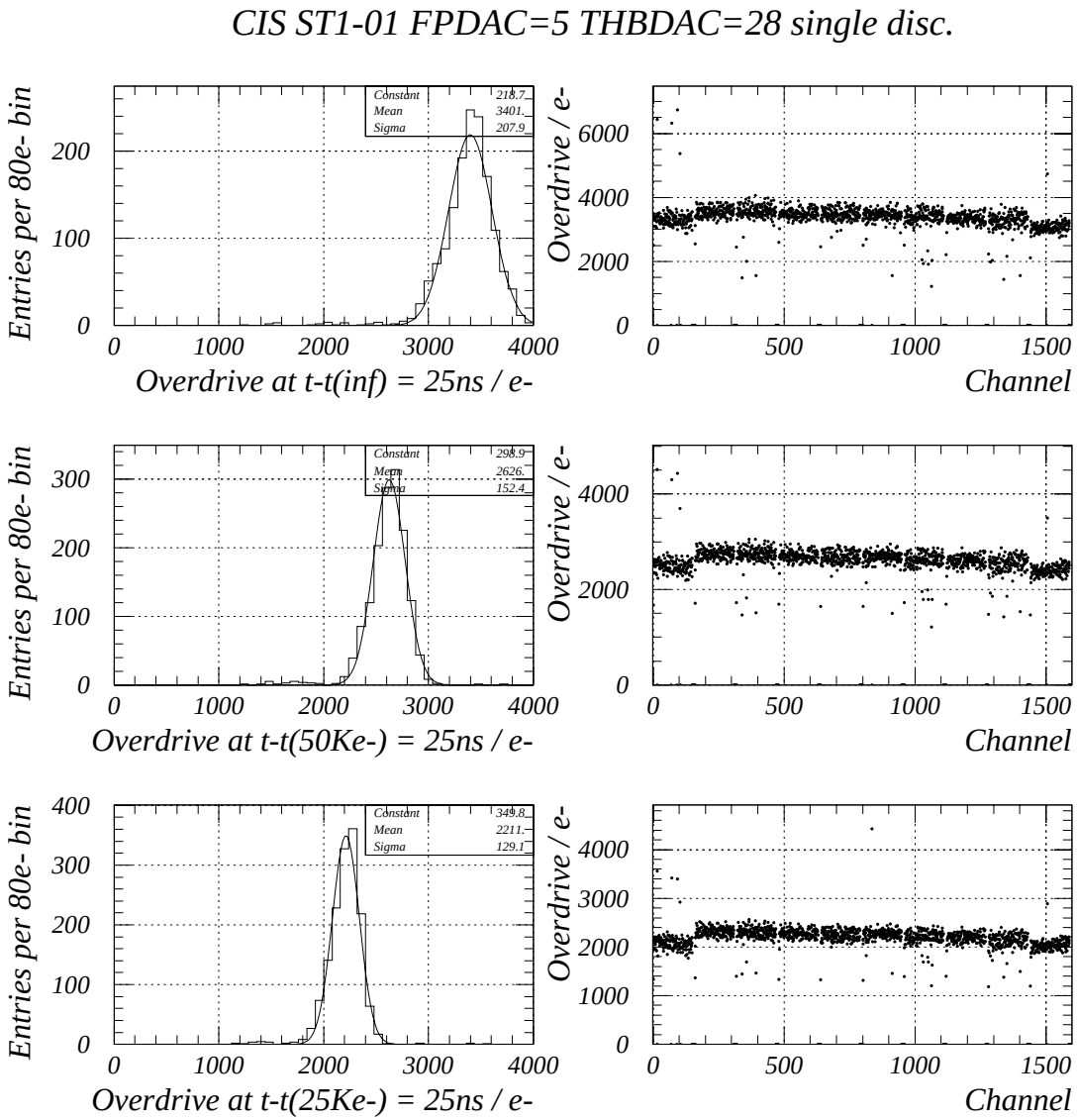

- Timing distribution for 2Ke overdrive has an RMS of only 1ns, and all channels of this particular chip appear at less than 25ns.
- This would imply a worst case in-time threshold of about 4Ke.

# Timewalk scan for ST1 detector at 3.5Ke threshold:



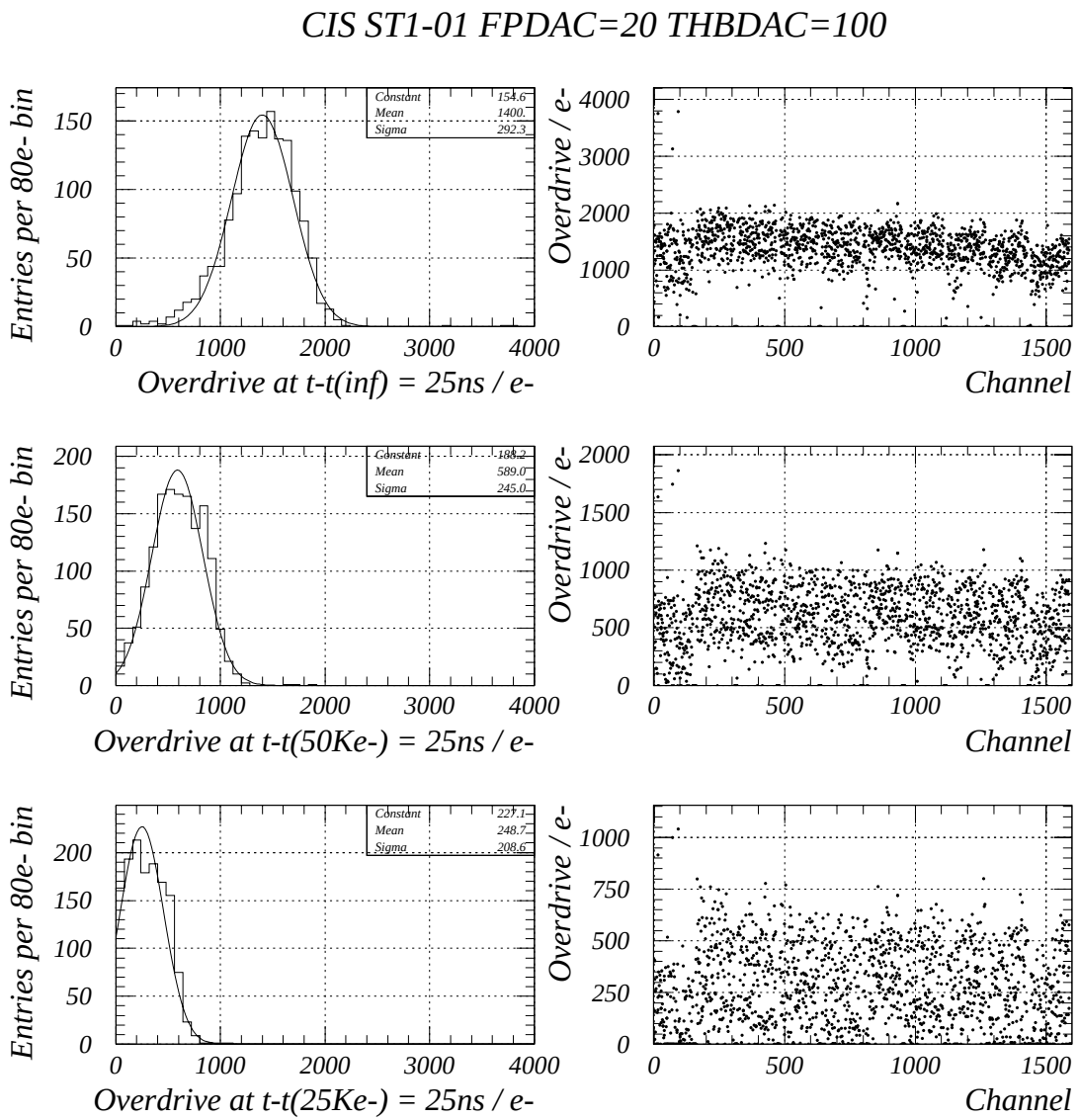

- Scan at higher threshold gives slightly worse performance, with a required overdrive of about 1.7Ke (referenced to 50Ke charge).
- This is consistent with the timewalk performance being independent of the THBDAC value.

# Performance in single discriminator mode, threshold 2.6Ke:



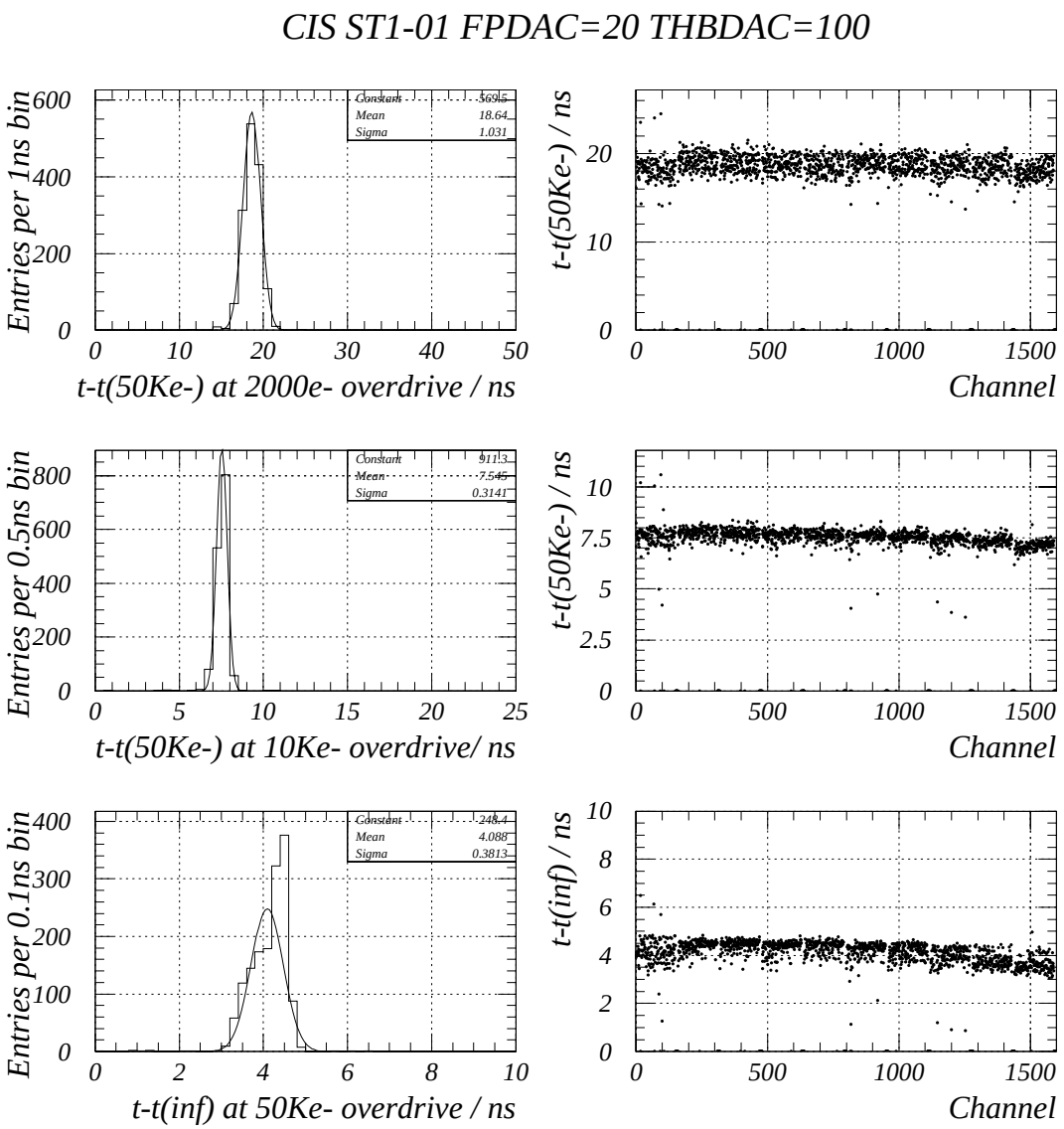

- Overdrive required for a 25 ns delay relative to the 50Ke reference charge is 2.6Ke.
- This is consistent with the dual-threshold overdrive plus the 900e nominal threshold separation for this operating point.

# Timewalk scan with 3.7Ke threshold and faster shaping:



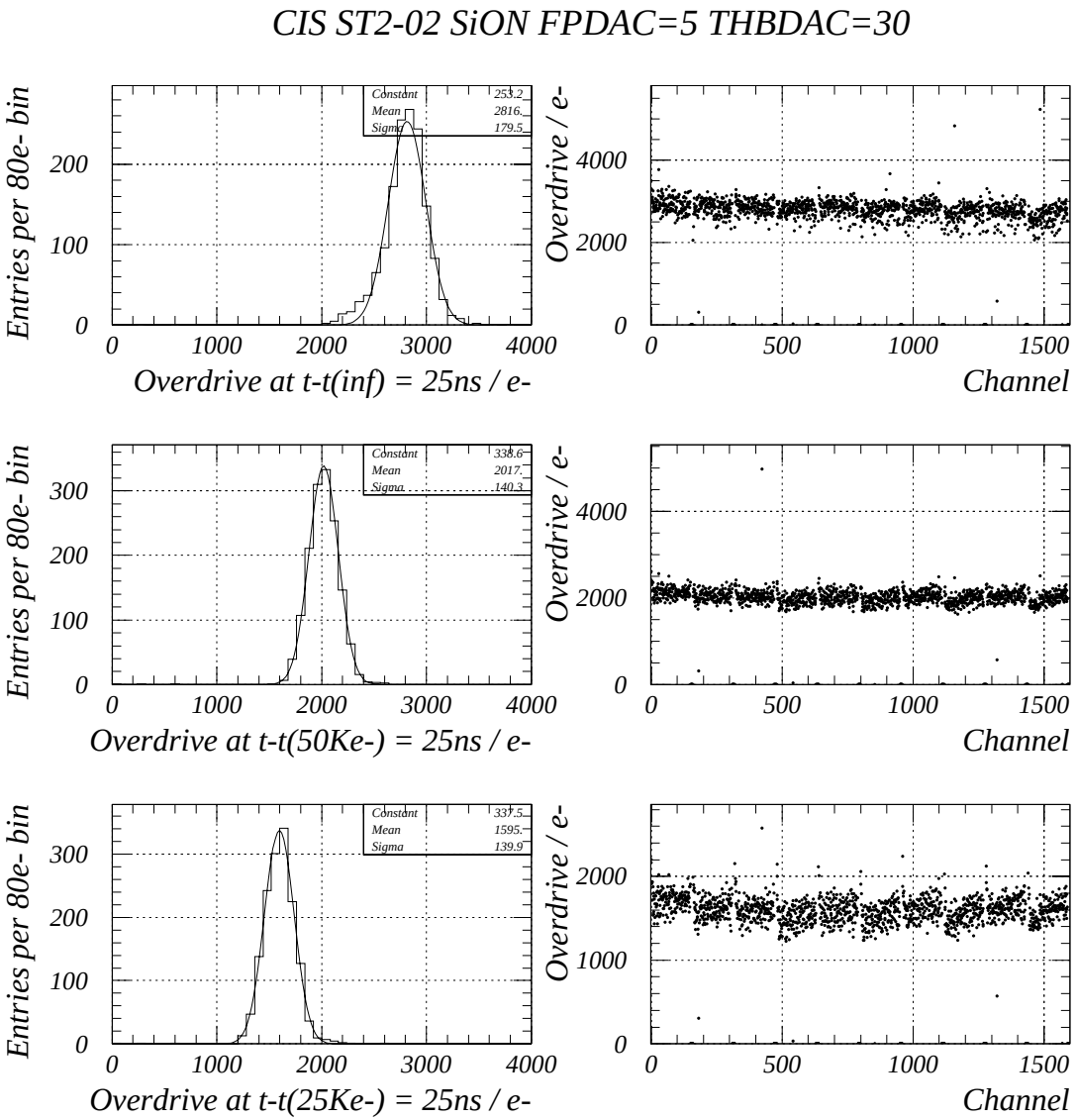

- Scan with roughly the same threshold and faster shaping (FPDAC=20).
- Observe a large improvement in the timewalk performance, with a required overdrive of only 600e instead of 1.7Ke.

# Detailed timing information for previous scan:



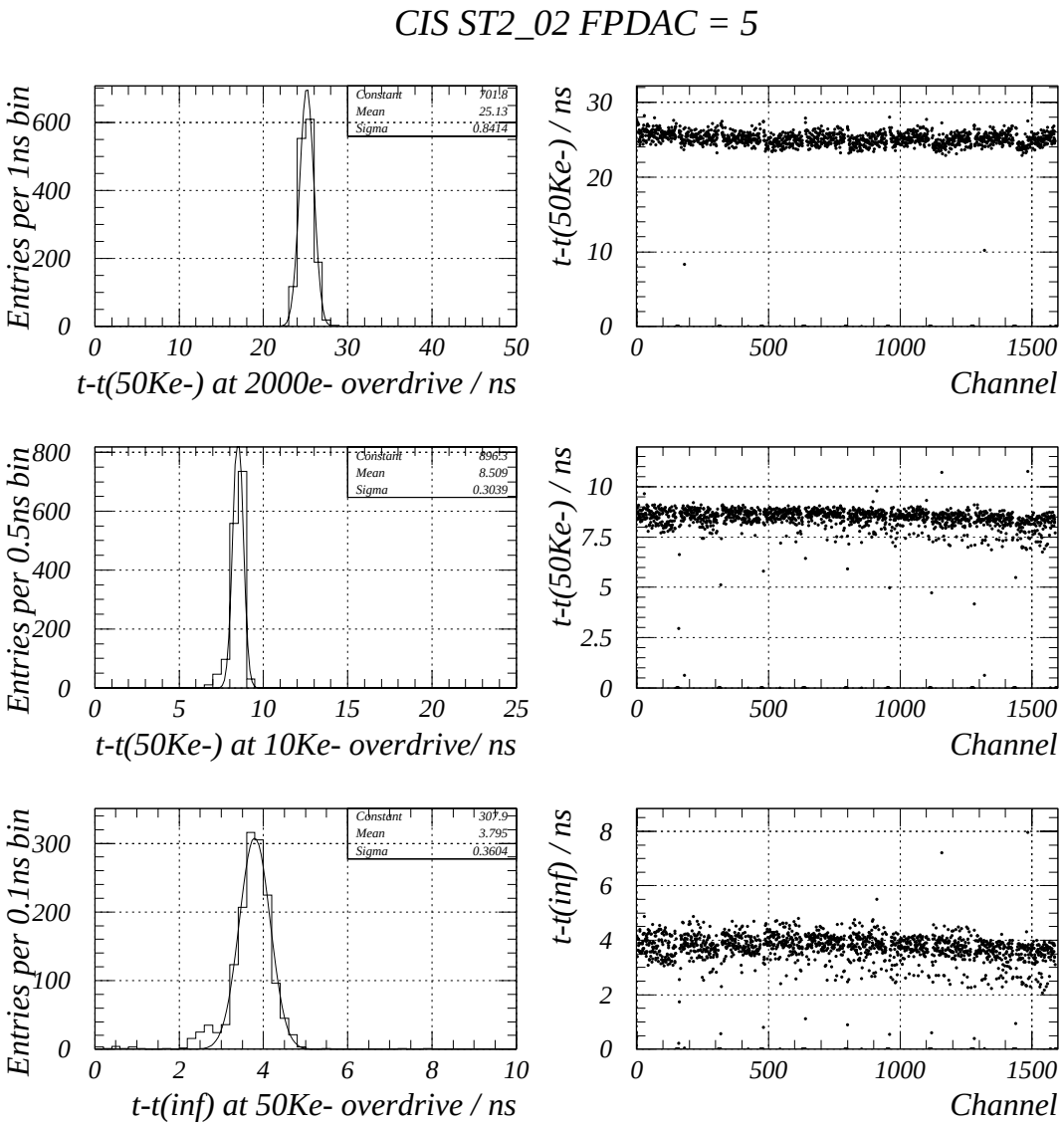

- Time difference distributions for different input charges. The charge has been corrected for the threshold for each pixel to get the overdrive.
- The channel to channel dispersion is quite low.
- Almost every channel has less than 20ns of delay relative to 50Ke input, for an overdrive of 2Ke.

# Timewalk scan for ST2, 3.2Ke threshold with slow shaping:



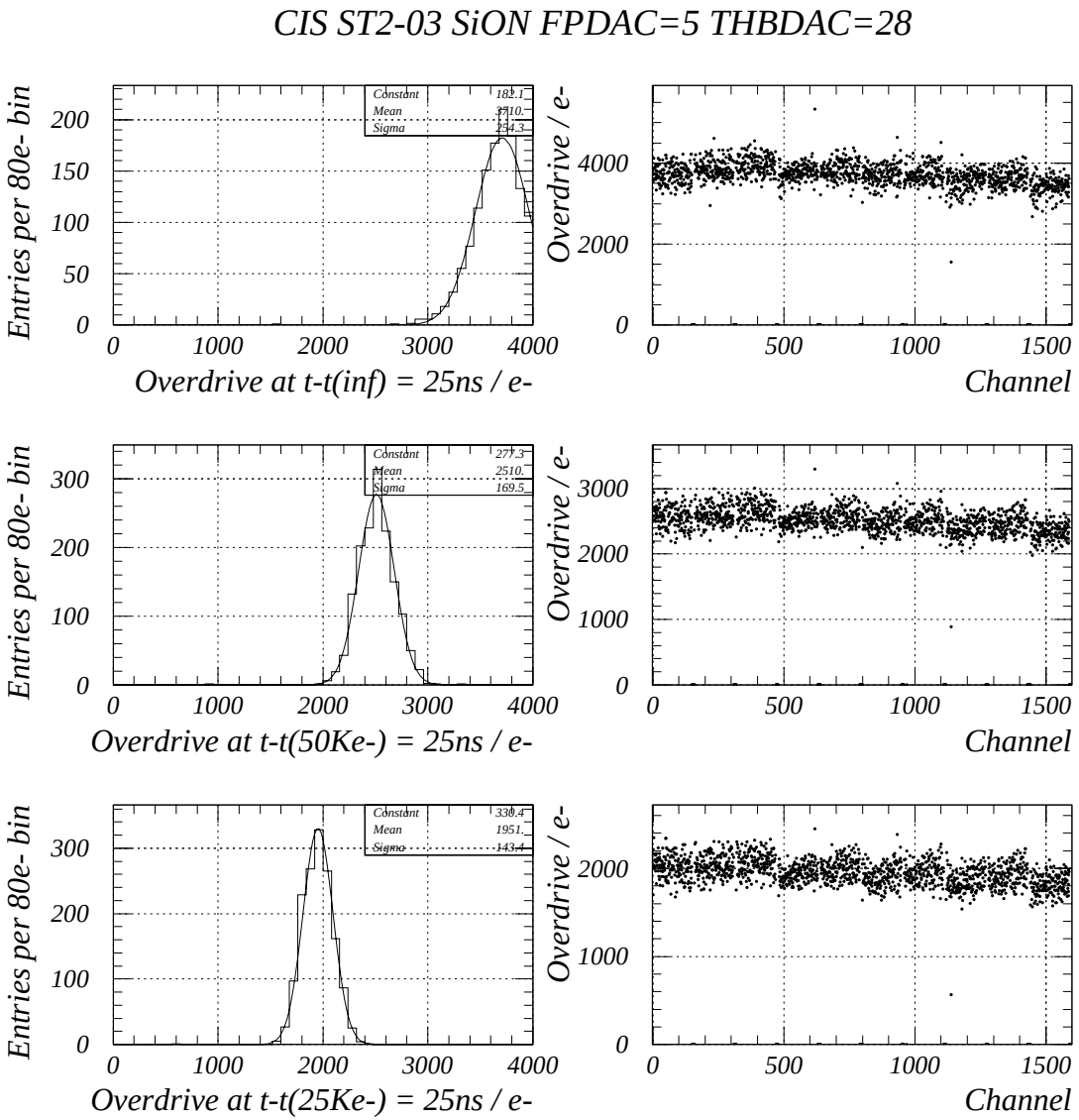

- Look at performance for an ST2 device.
- With slow shaping, observe an overdrive of 2.0Ke is necessary for a 25ns delay relative to a 50Ke reference input.

# Look at detailed timing for this scan:



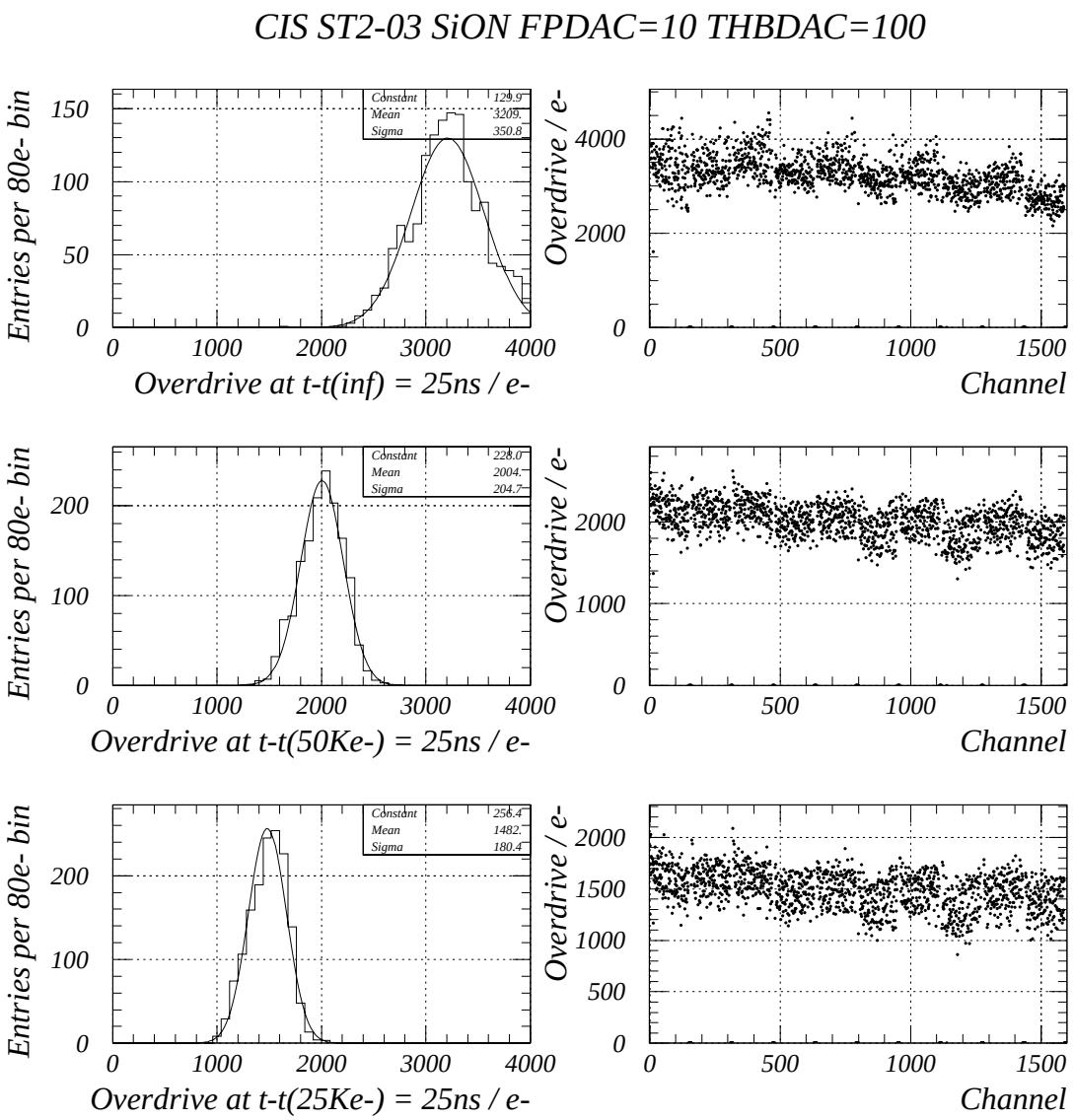

- With a 2Ke overdrive, the mean delay is 25.1ns relative to the reference charge of 50Ke.
- This is about 1.5ns more than for the equivalent operating point of the ST1 device.

# Perform scans of a second ST2 device:



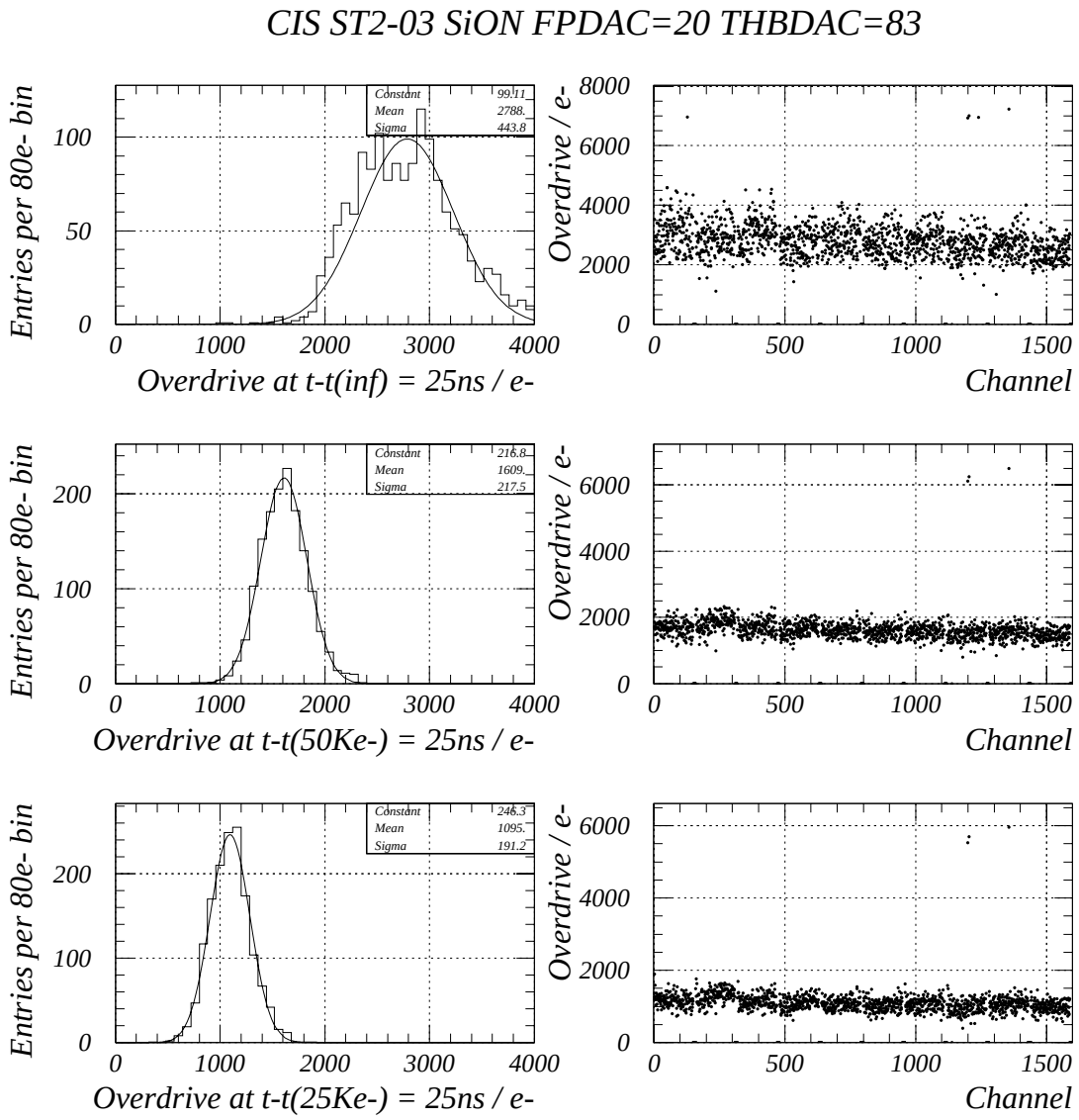

- Scan with FPDAC=5 and threshold of 3.2Ke.
- Find a required overdrive of 2.5Ke for 25ns delay.
- The detailed timing distribution gives a delay of 27.8ns for 2Ke input charge.
- This is about 4ns more than for the equivalent ST1 device, and appears to be larger than the expected variation.
- Given the strong dependence on FPDAC, this could arise if the shaping time differs, although the chips used the same FPDAC value.

# Perform a scan with FPDAC=10:



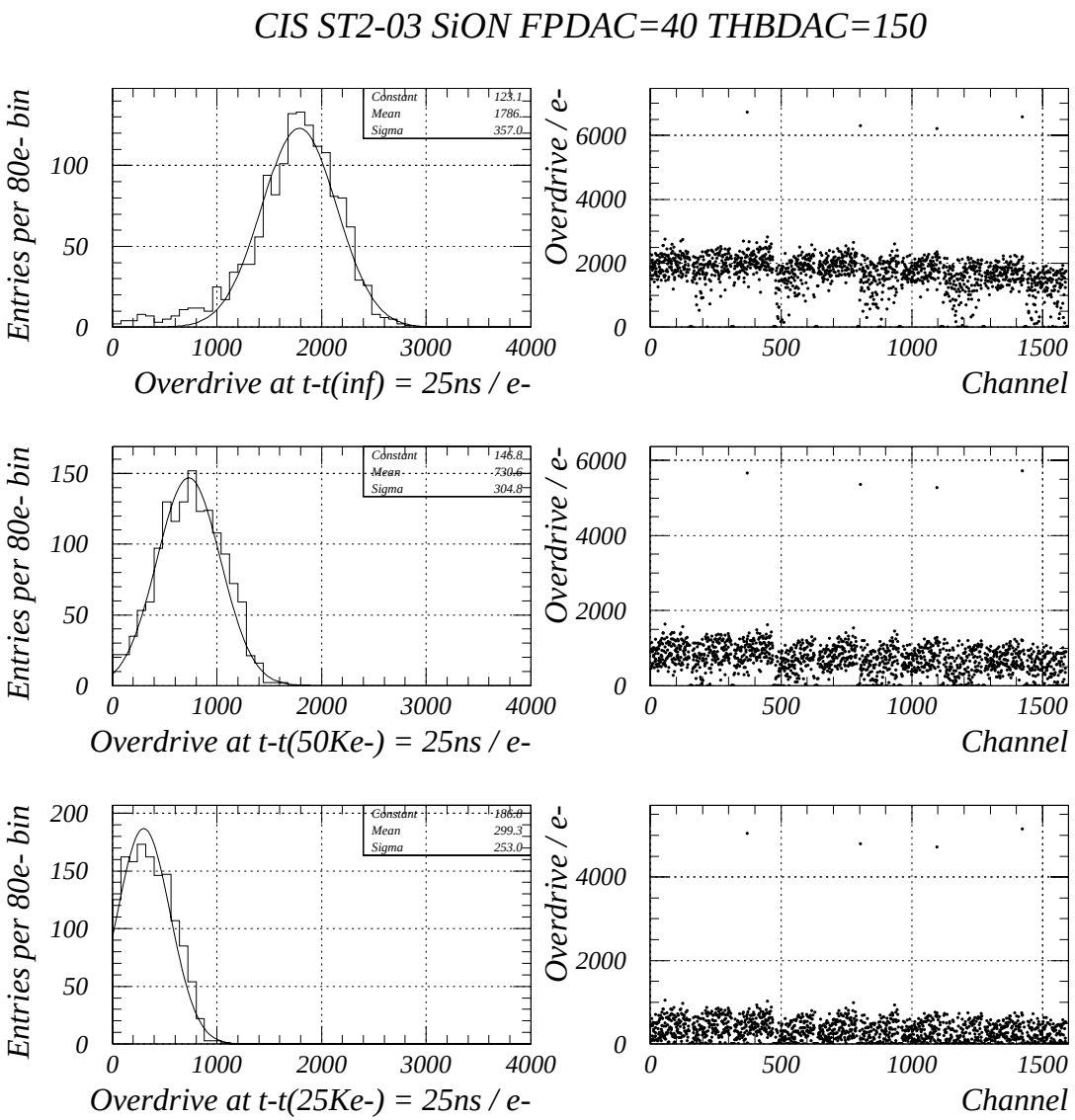

- The threshold for this setting is 2.7Ke.
- With slightly faster shaping, the required overdrive is reduced to 2.0Ke.
- The corresponding delay for 2Ke overdrive is 25.0ns as expected.

# Perform a scan with FPDAC=20:



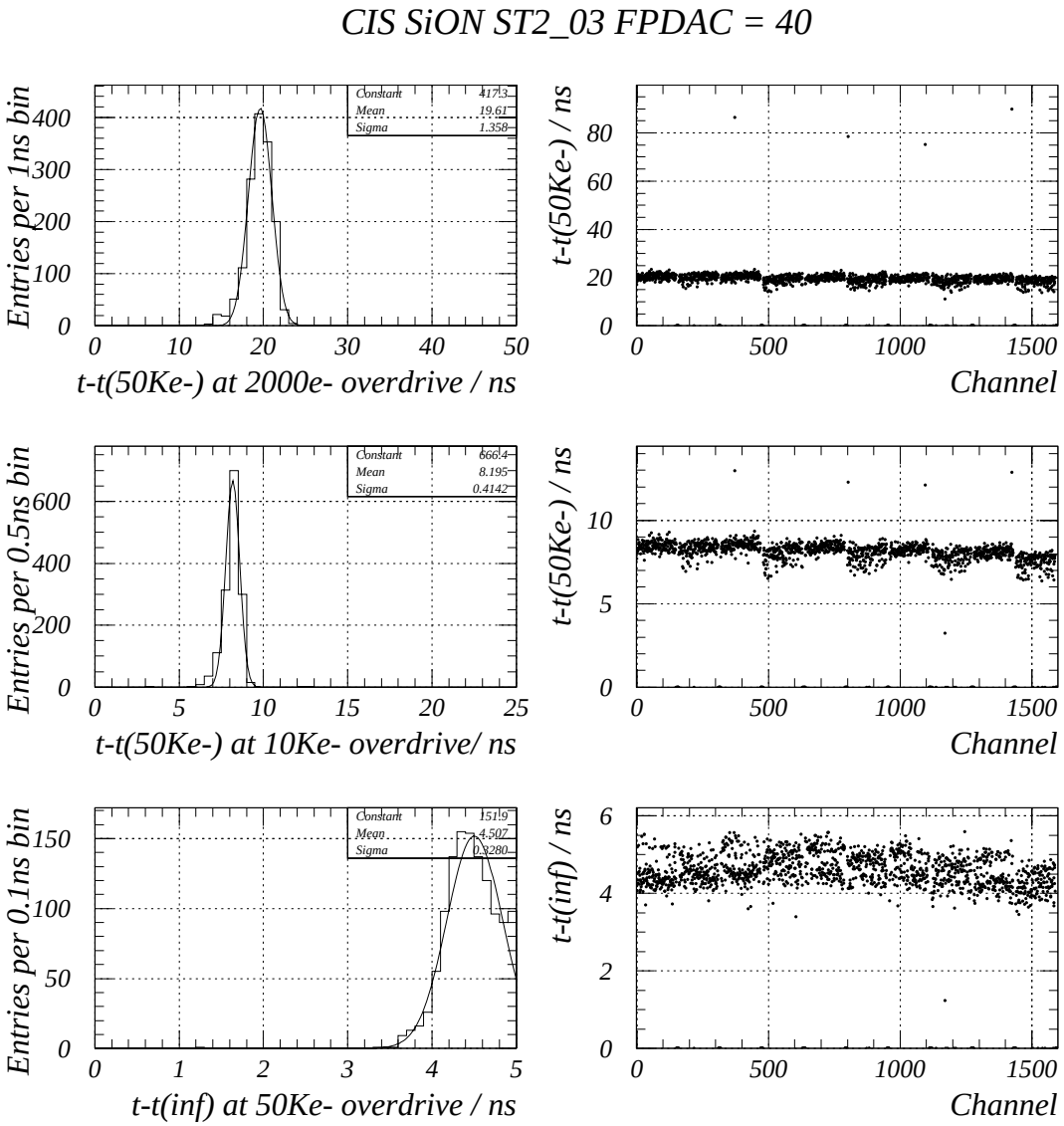

- The threshold for this setting is 3.5Ke.
- With this shaping, the required overdrive is reduced further to 1.6Ke
- The corresponding delay for 2Ke overdrive is 23.2ns

# Perform scan for FPDAC=40:




- This setting has a threshold of 3.5Ke, and a noise of 200e.
- The required overdrive is 730e to achieve the 25ns delay specification.

# Detailed timing distributions for this scan:

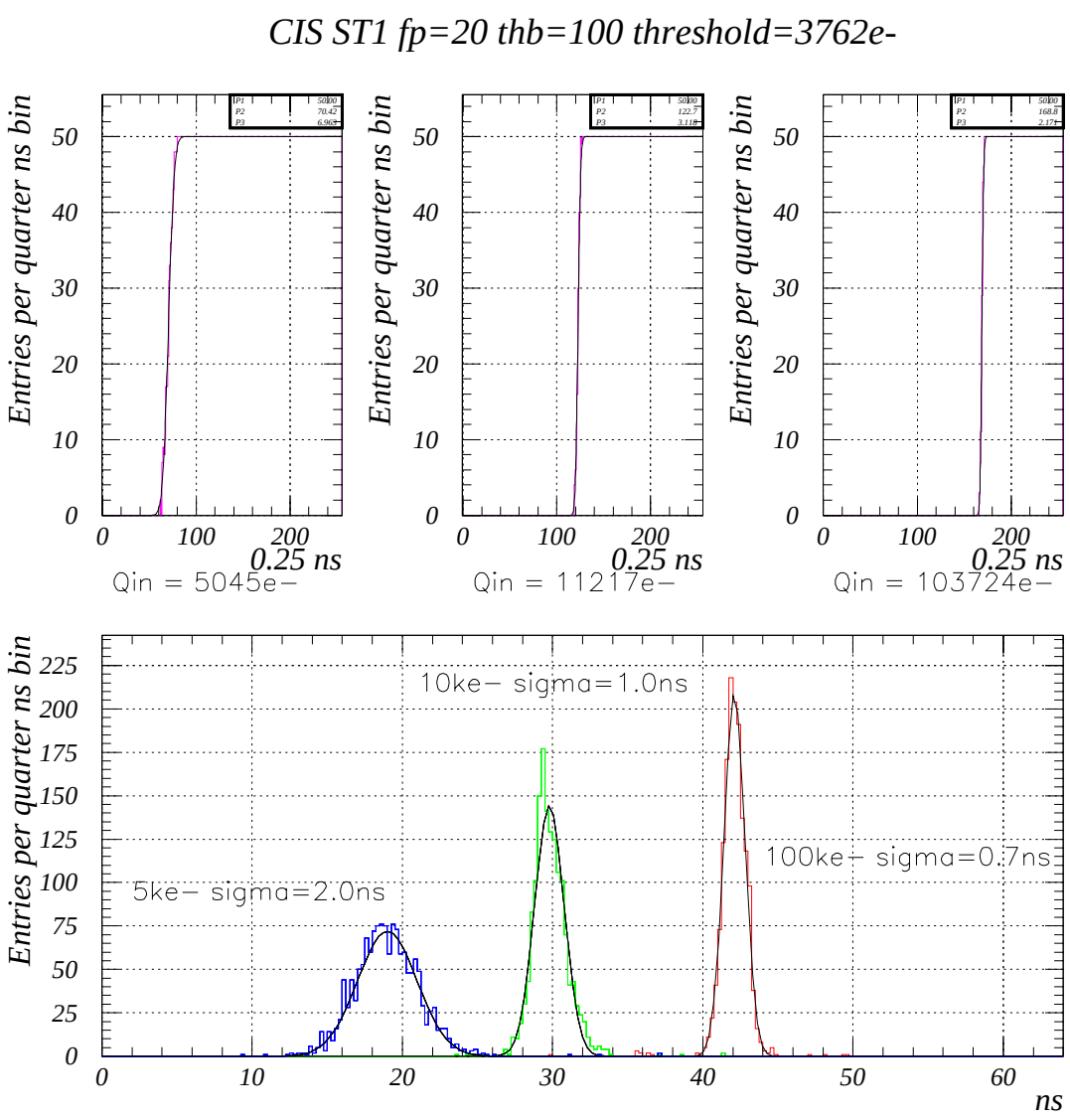



- Distribution of time delays for this setting shows a mean delay of 19.6ns for an overdrive of 2Ke.
- In this case, essentially all channels arrive with a delay less than about 22ns.

# Further considerations:

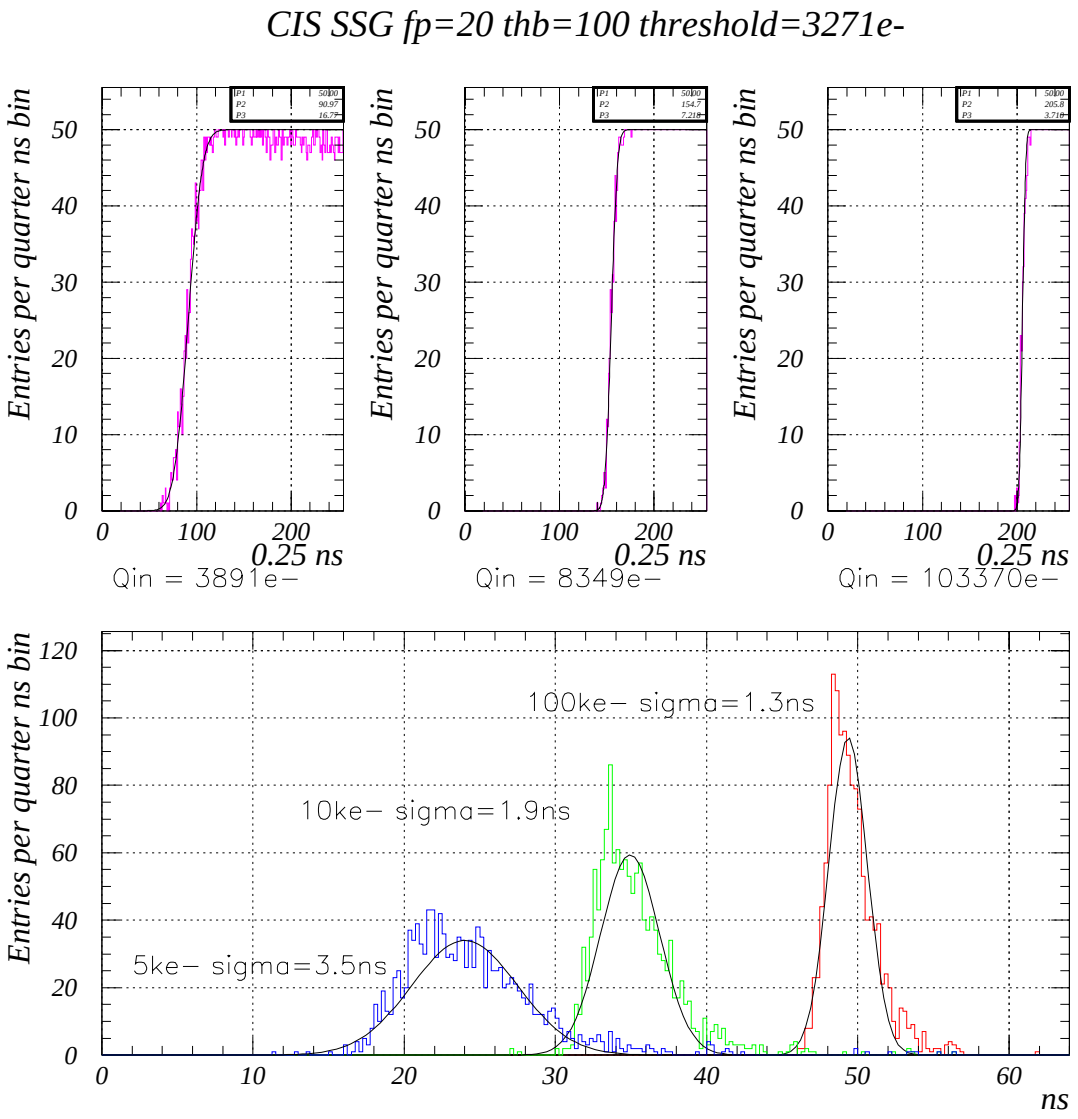
- We have not yet defined a precise specification of the timewalk requirements for ATLAS pixels. However, it would seem reasonable to attribute only about 20ns of the available 25ns to the FE chip timewalk contribution. Additional contributions will arise from the ability to adjust the 40 MHz clock arrival time at each module, as well as from dispersion within individual chips.
- A detailed algorithm to “time in” the detector must be defined. An example could be to require that accepting 95% of the hits created by injecting 50Ke charge into the FE chip would define the “$t_0$”. The “in-time efficiency” would be given by the minimum charge such that 95% of the corresponding hits would arrive within 20ns of this “$t_0$”. This definition would cover both the jitter and noise aspects of single channel performance, as well as overall dispersion effects within a chip and a module.
- With such a definition, one can then define a maximum acceptable “in-time threshold”, which defines the timewalk performance required of the FE chip. This definition will be at least 1-2ns more conservative than simply requiring the mean delay to be less than 20ns.
- Further detailed studies are required to clarify the precise definition, and to better understand the variation between chips that has been observed so far. We also need to carry out scans of irradiated detectors to verify the performance in the presence of leakage current.

# Absolute time distributions for an ST1 scan:




- Three S-curves versus strobe delay are shown for a typical channel. The left plot has sigma of 2ns.
- The lower curves show the distribution of the fitted mean (50% point) for such curves for all channels on the ST1 assembly.
- The channel to channel dispersion on the 50% point is fairly small
- However, the width of the distribution for a single channel is comparable, especially for smaller charges. This width is greater than expected from the measured noise.

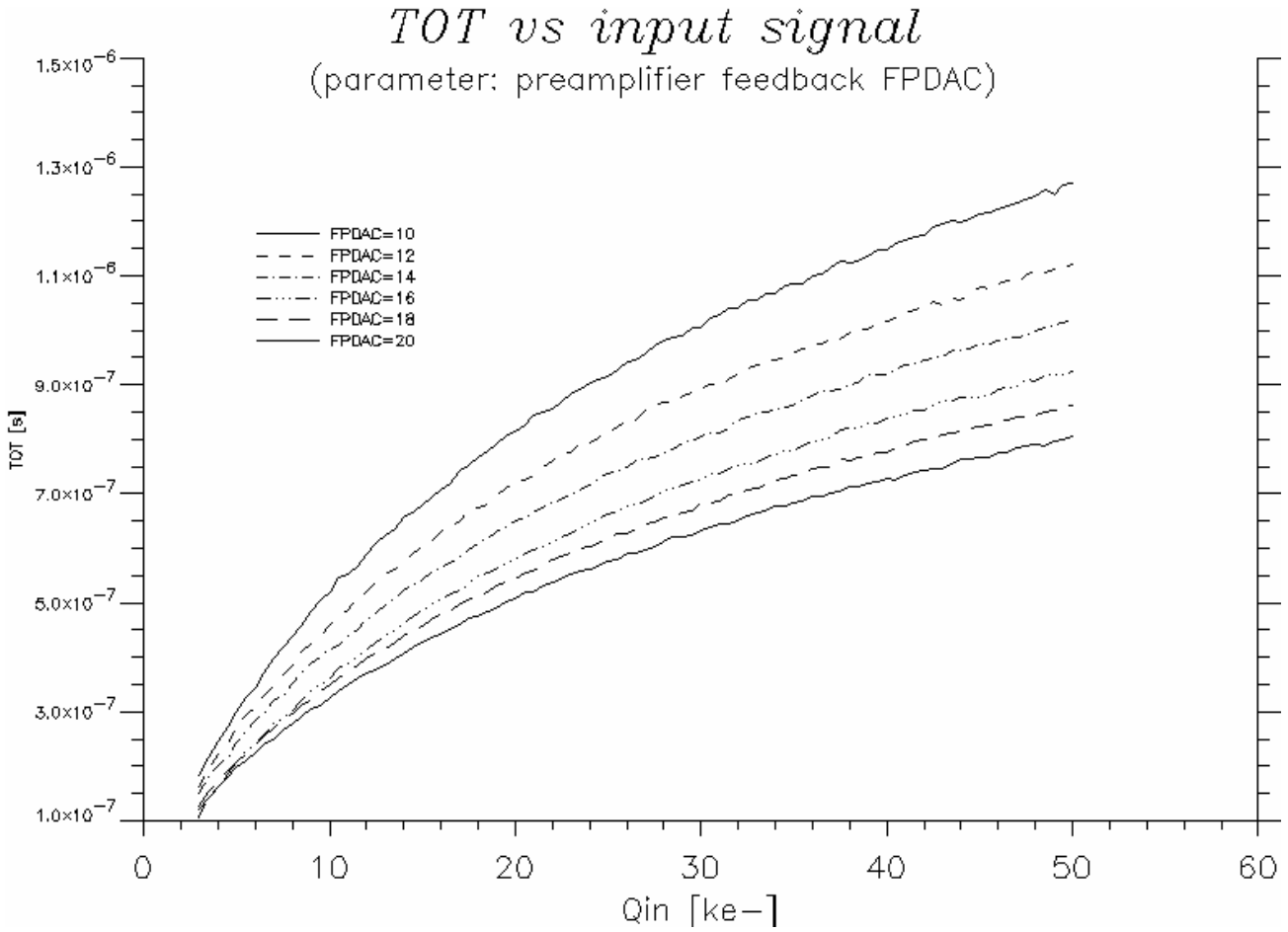
# Absolute time distributions for an SSG scan:




- This assembly shows poorer timewalk performance, most likely because of differences in the actual TOT for a given FPDAC.
- The single channel fluctuations for small input charge are 4ns RMS
- The overall dispersion, using the 50% point on each channel, is similar.

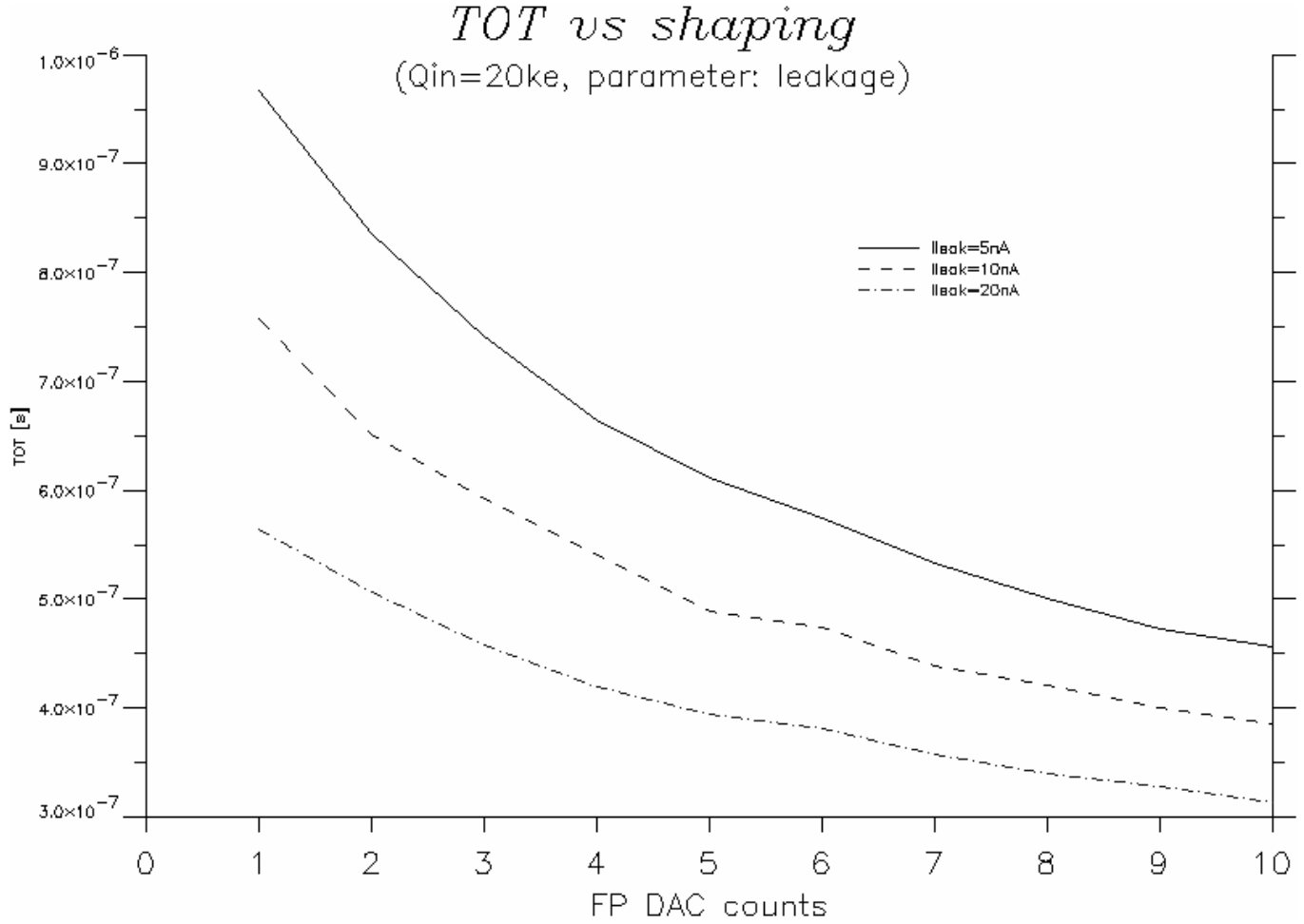
# TOT Behavior

## Dependence of TOT on feedback current:



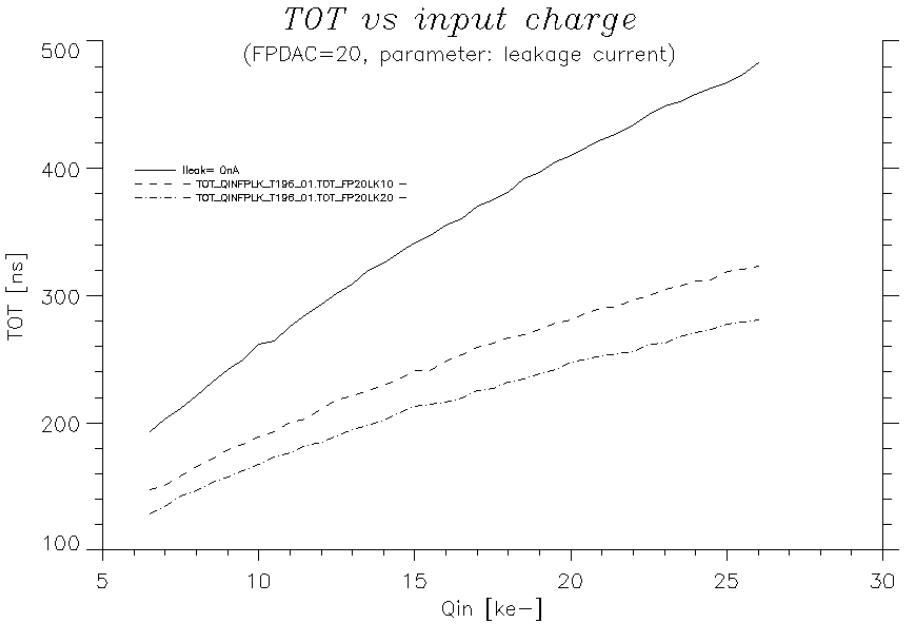

- Roughly 500 ns TOT for 20 Ke charge with FPDAC=20 (normal value). Increases to 800 ns TOT if FPDAC=10. This is without significant leakage current.

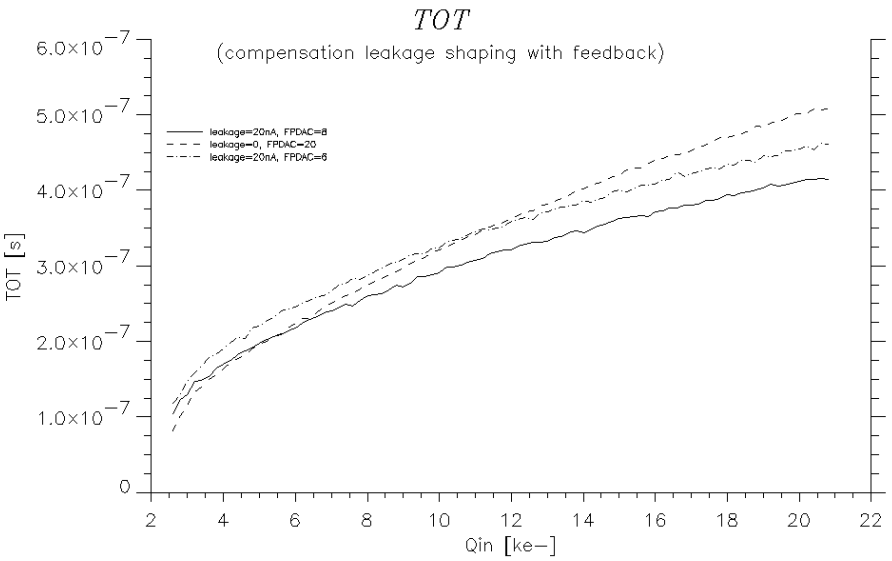
# Dependence of TOT on leakage current:




Shaping time of the preamplifier changes significantly with leakage current.

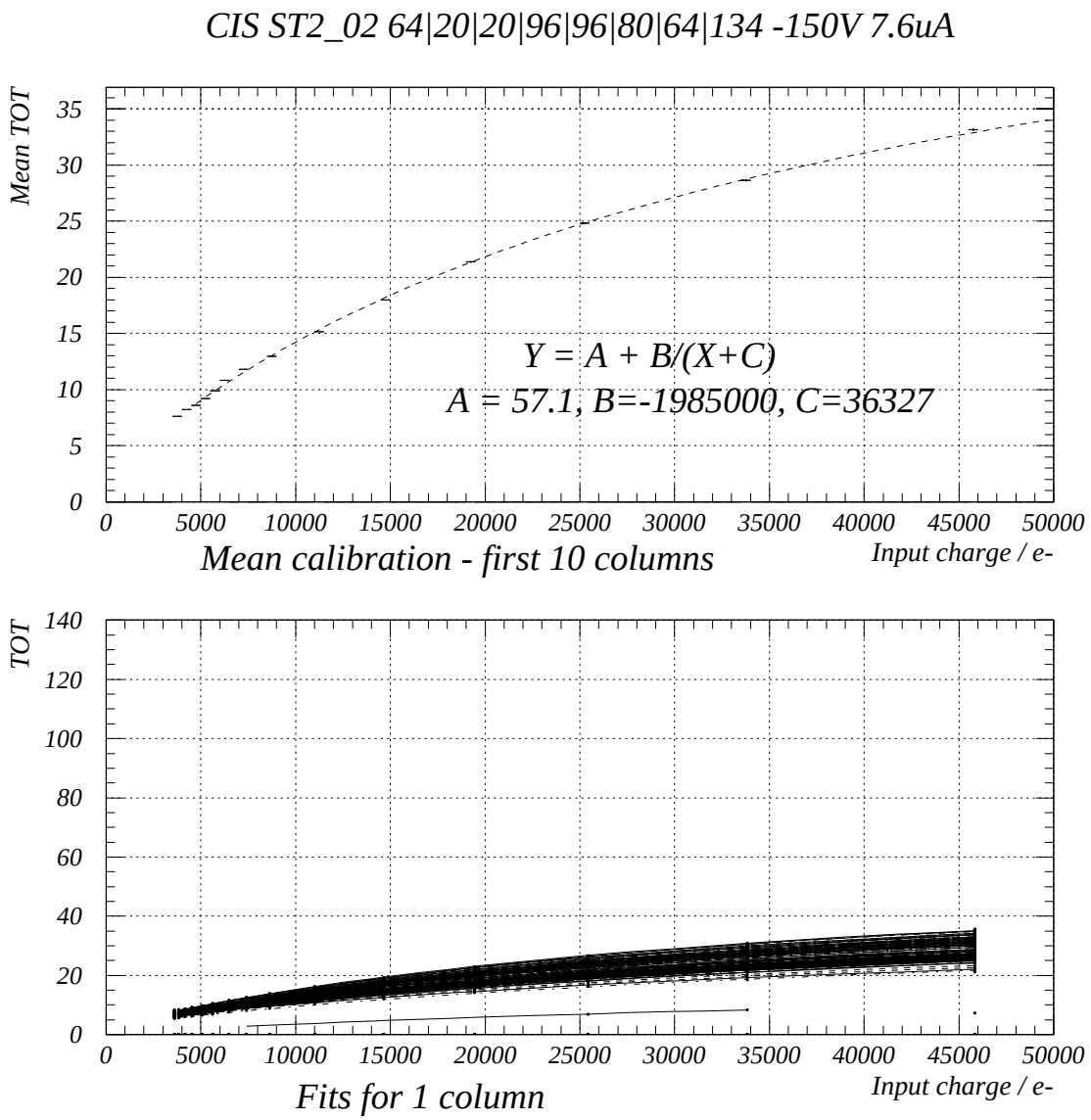
# Compensation of leakage current by feedback current:



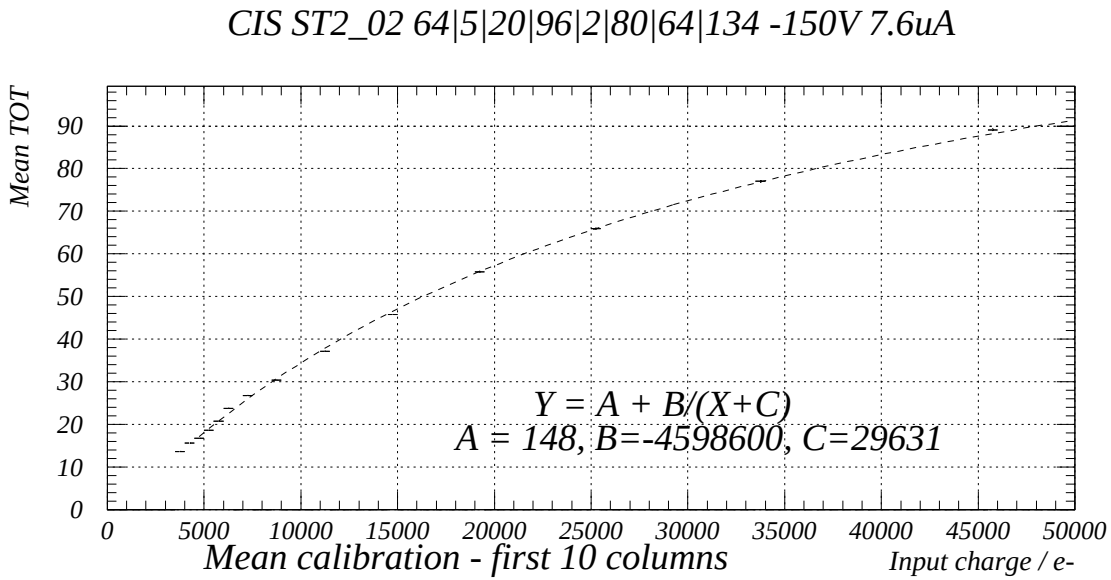

- Response curve changes shape slightly, but the major effect can be compensated by reducing the feedback current for a non-zero leakage current.
- For a 20 nA/pixel leakage, the original response with FPDAC=20 can be approximately recovered by reducing FPDAC=5.
- It is not possible to significantly extend the return to baseline time in the presence of large leakage current (turning off the feedback current altogether doesn't even help). Hence to get good resolution charge measurements on heavily irradiated detectors, they must be very cool to reduce the leakage current (-30 C).

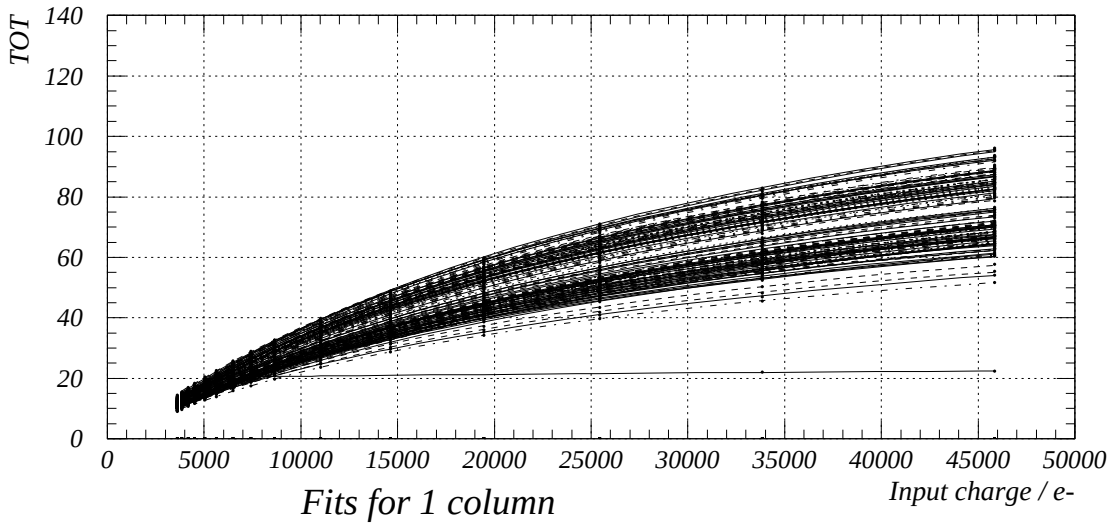
# Sample TOT calibration scan for ST2:




- This scan uses a non-uniform list of charges to explore the complete transfer function.
- This ST2 detector had FPDAC=20, which gives roughly 500ns return to baseline time for a 20Ke input charge.
- The upper plot averages over all pixels.
- The lower plot shows the level of TOT dispersion.
- The cutoff at low TOT values is due to the dual-threshold mode. In single discriminator mode, the TOT extends down to values of zero.

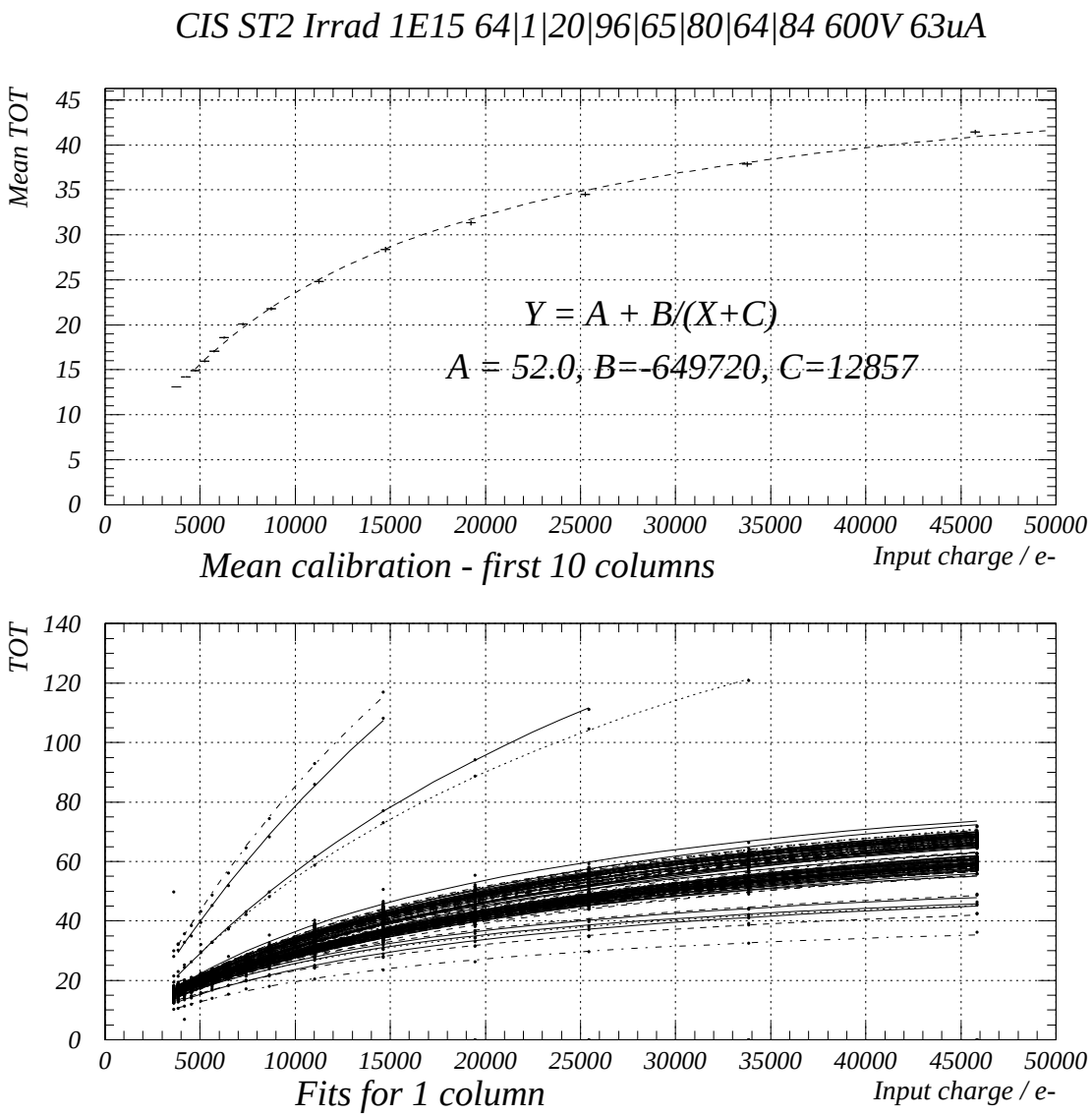
# TOT scan with reduced feedback current:



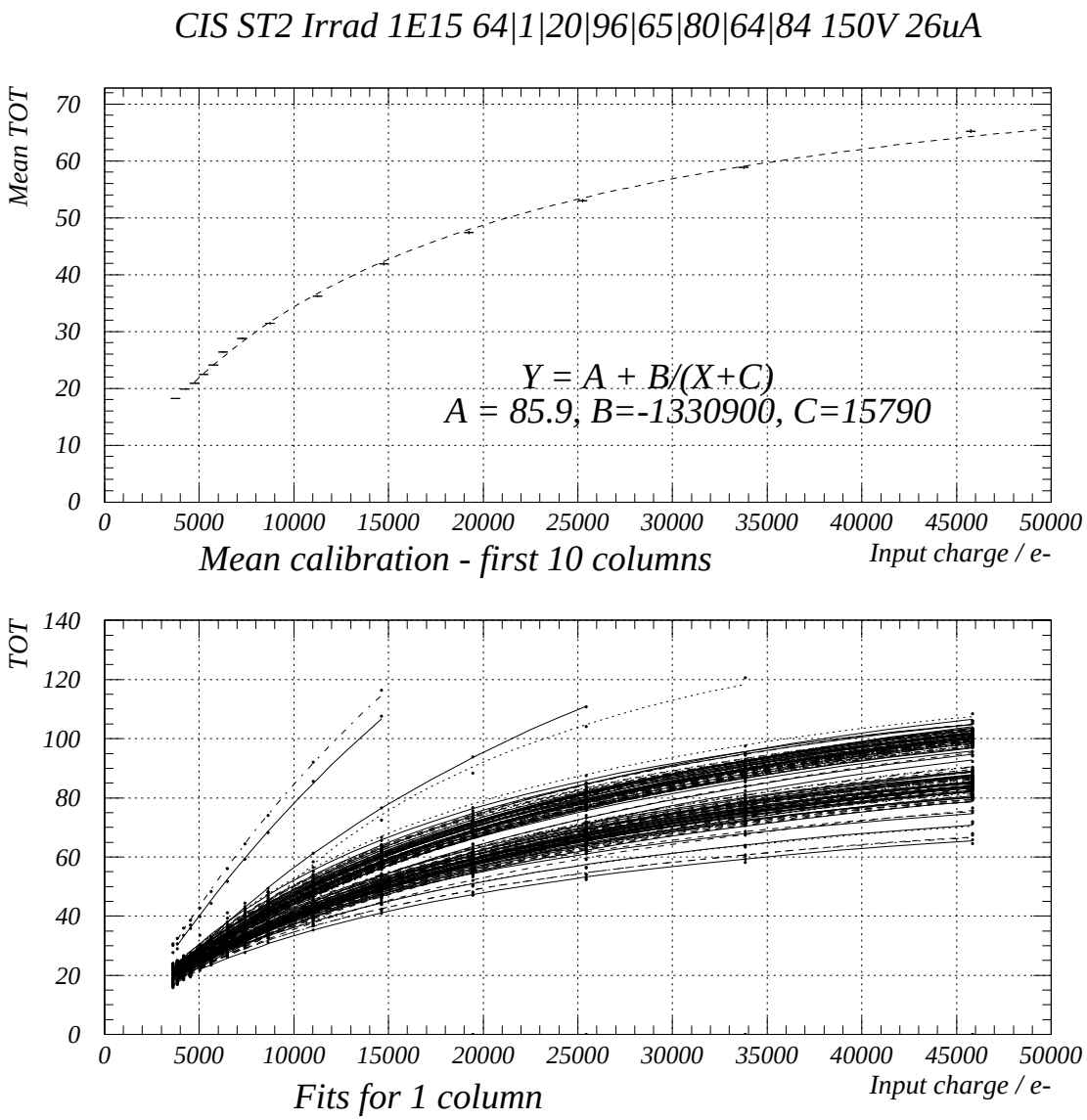

- By reducing FPDAC from 20 to 5, the shaping time is increased by roughly a factor of three.
- The return to baseline for a 20Ke input charge is now about 1.5 µs.
- This still provides quite safe operation for a latency of 2.5 µs (hits with a trailing edge after the L1 latency will fail to satisfy a trigger coincidence and will be lost in FE-B).

# TOT scan with leakage current:



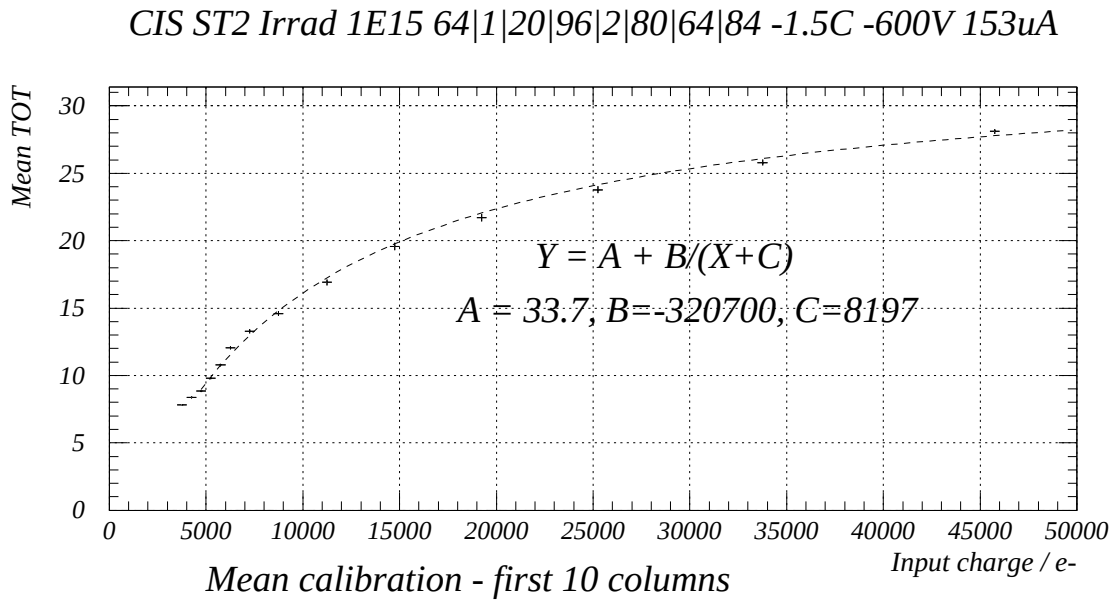

- Measure TOT performance for irradiated detector with 63 µA of leakage (about 22 nA/pixel) at 600V.
- Reduce FPDAC to minimum setting to get best possible TOT measurement.
- With this leakage, can stretch return to baseline to about 1000ns for 20 Ke.
- Note the detector itself only gives about 10Ke for a MIP track with this bias voltage.

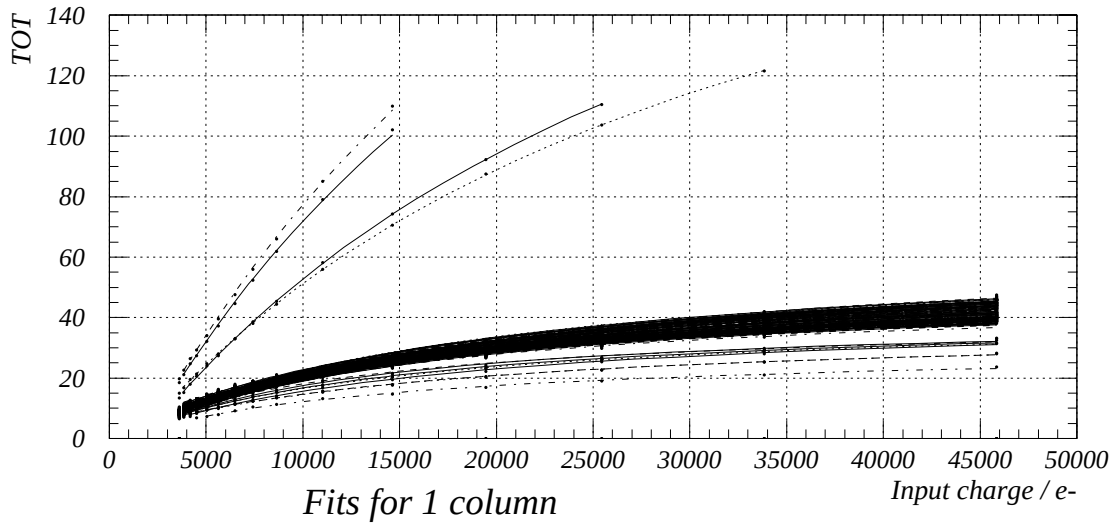
# TOT scan with smaller leakage current:




- Operation of detector at reduced bias of 150V reduces leakage to 26 µA, or about 10 nA/pixel.
- This increases the return to baseline for 20Ke to about 1.5 µs.
- Note however that the detector is very partially depleted and would only give about 6Ke of charge for a MIP.

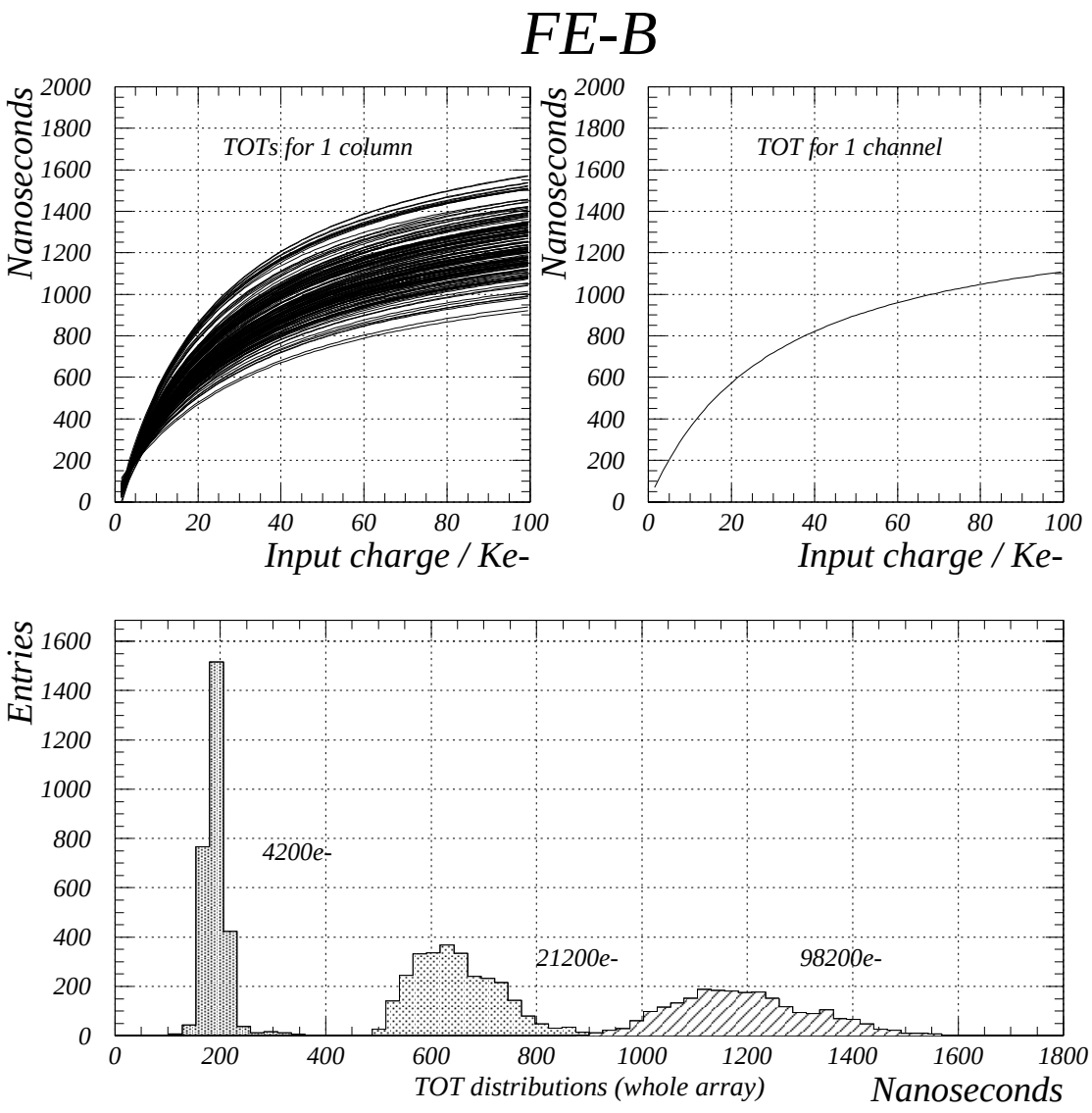
# TOT scan with larger leakage current:




- Operation of the detector at increased temperature increases the leakage current to 153 µA, or about 50 nA/pixel.
- This reduces the return to baseline time to about 500ns for 20Ke of input charge.

# TOT dispersion:



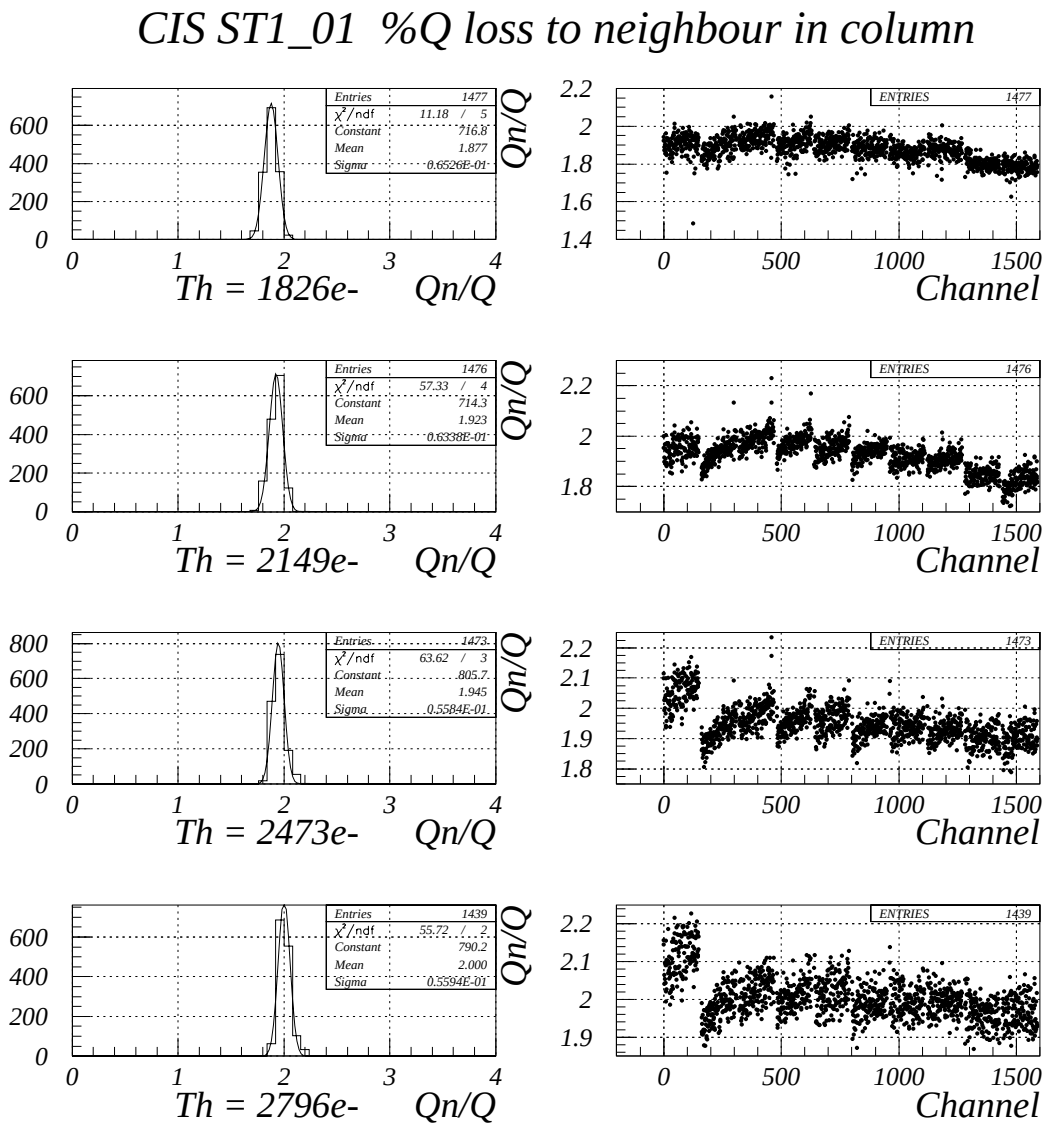

- Upper left plot shows TOT curves for single column (160 pixels).
- Dispersion observed has large odd/even row component.
- Dispersion thought to arise from matching problems in the “return to baseline” circuitry in diff-amp.
- This is only place it can occur without increasing the threshold dispersion.
- With the present design, things can be improved, but it is hard to eliminate.

# Cross-coupling Measurements

## Measure rejection against signal on one pixel firing neighboring pixels:

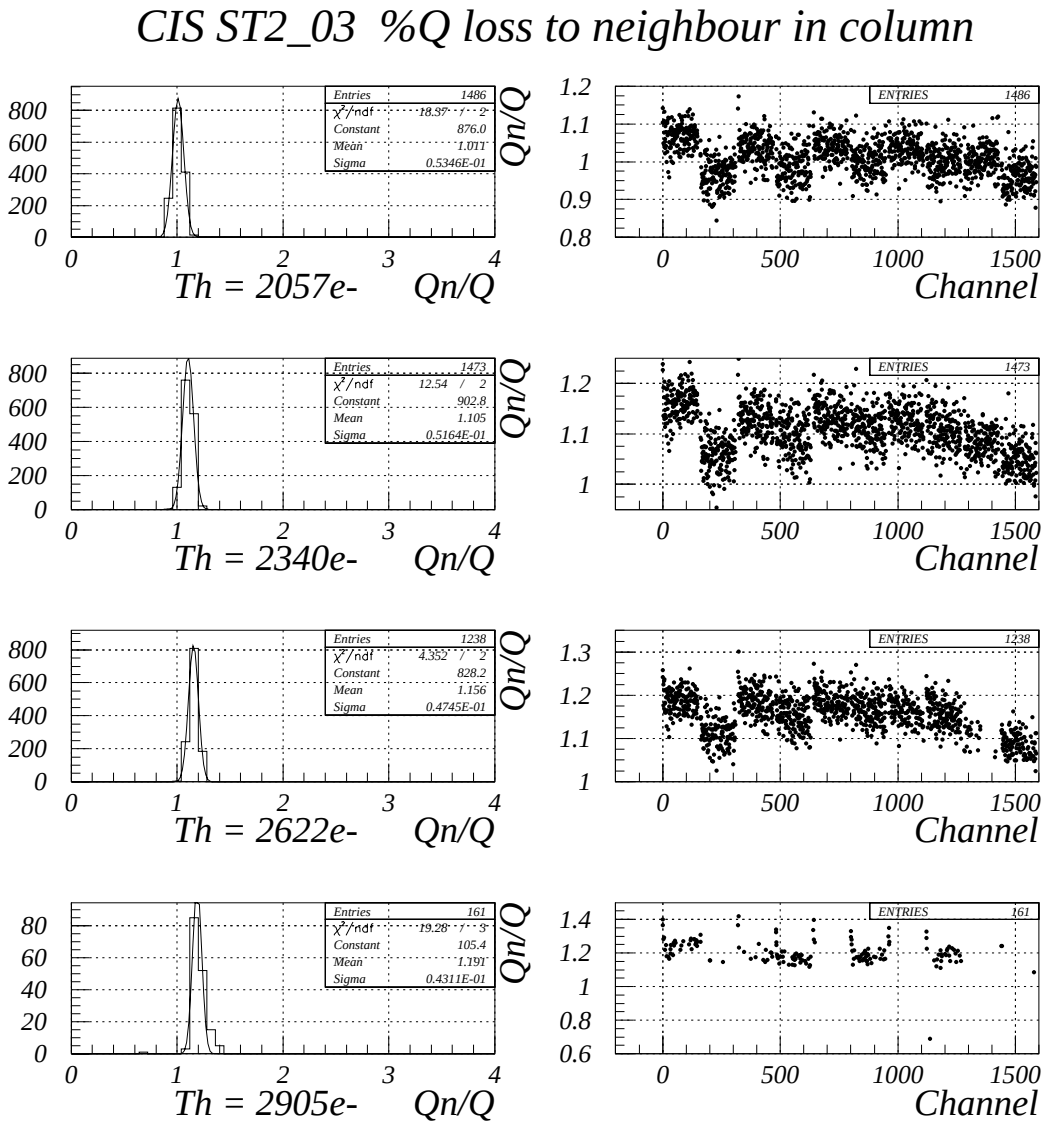
- Principle mechanism for coupling is inter-pixel capacitive coupling. Other couplings such as inter-bump capacitive coupling should be much smaller.
- Basic measurement technique is to inject charge on one pixel (but not read it out) and read out the nearest neighbors.
- The largest cross-coupling should occur to the “row neighbors” directly above and below the injected pixel.
- Additional studies have been done to look at column neighbors. It is observed that no crosstalk is measurable between column neighbors that are not “bump neighbors” (for example, column 0 and 1 are not bump neighbors, but column 1 and 2 are). A small coupling is seen to those neighbors which have a bump within one row of the injected pixel.
- This technique is limited by the magnitude of the charge that can be injected. This is determined by the maximum VCal that can be applied prior to diode clamping (about 4V) on a 10 fF injection capacitor, or about 240 Ke. Note that for this case, the possible parasitic coupling of the VCal line itself to the inputs of non-injected neighbors could be a problem. In FE-B, non-injected pixels have their injection capacitor grounded by a switch so there should be little coupling of this kind.

# Cross-coupling in ST1 detector:




- Express ratio of threshold to input charge as a percentage (2% means 100Ke input charge is required to fire a 2Ke threshold).
- Find column 0 has higher crosstalk (enhanced coupling due to presence of guardring on detector ?)
- Approximate level of crosstalk is 1.9%.

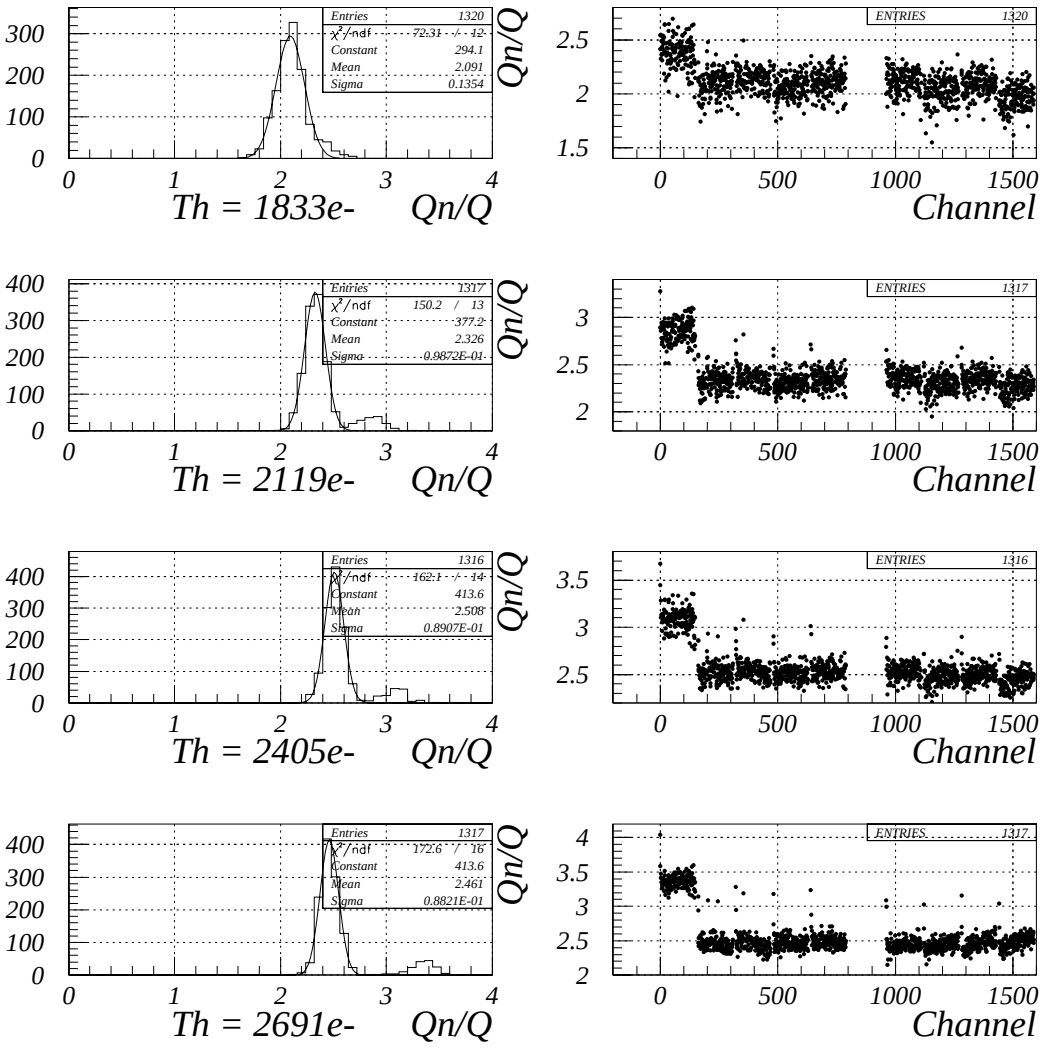
# Cross-coupling in ST2 detector:




- Observe lower cross-coupling in ST2 detector design, presumably due to presence of floating n-ring which reduces the interpixel capacitance.
- Approximate level of crosstalk is 1.1%

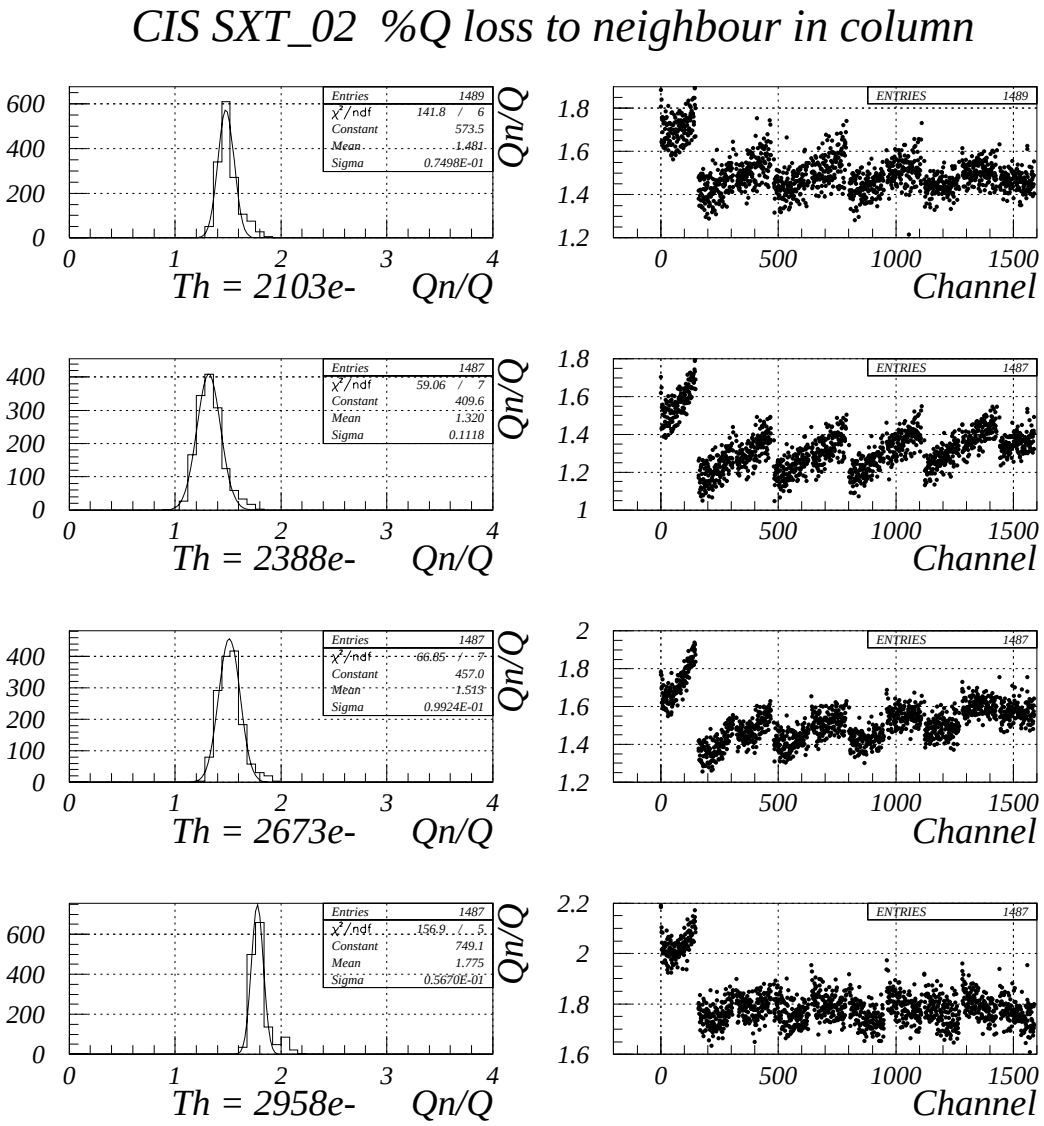
# Cross-coupling in SSG detector:

*CIS SSG_01 %Q loss to neighbour in column*



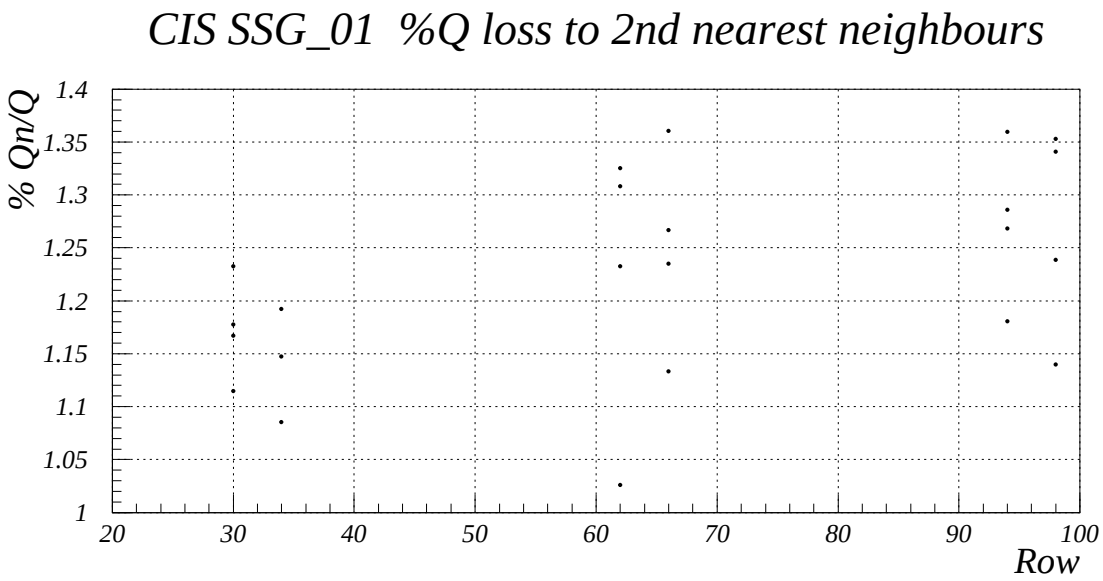

- This detector design has the highest inter-pixel capacitance due to its narrow gaps.
- Approximate level of crosstalk is 2.3%

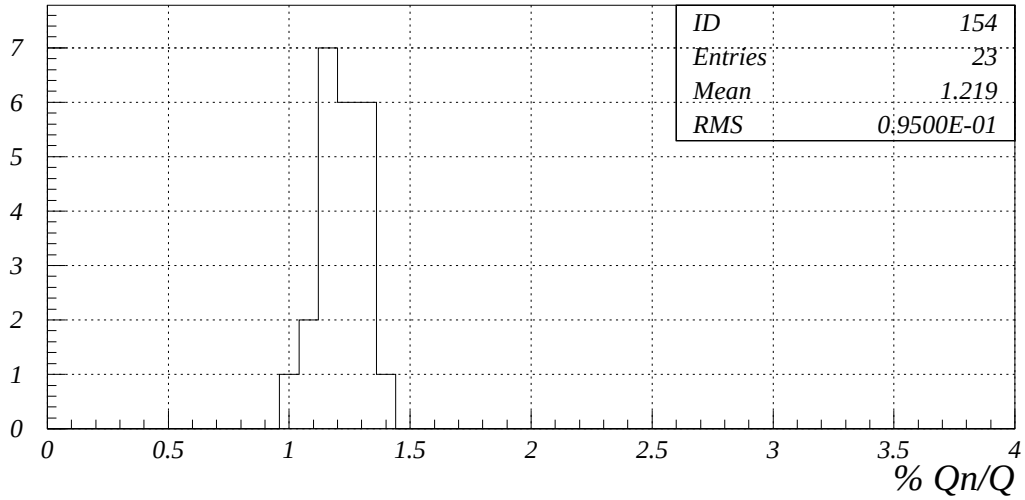
# Cross-coupling in SXT detector:




- This detector design has a higher total capacitance than SSG, but a lower inter-pixel capacitance.
- Approximate level of crosstalk is 1.5%

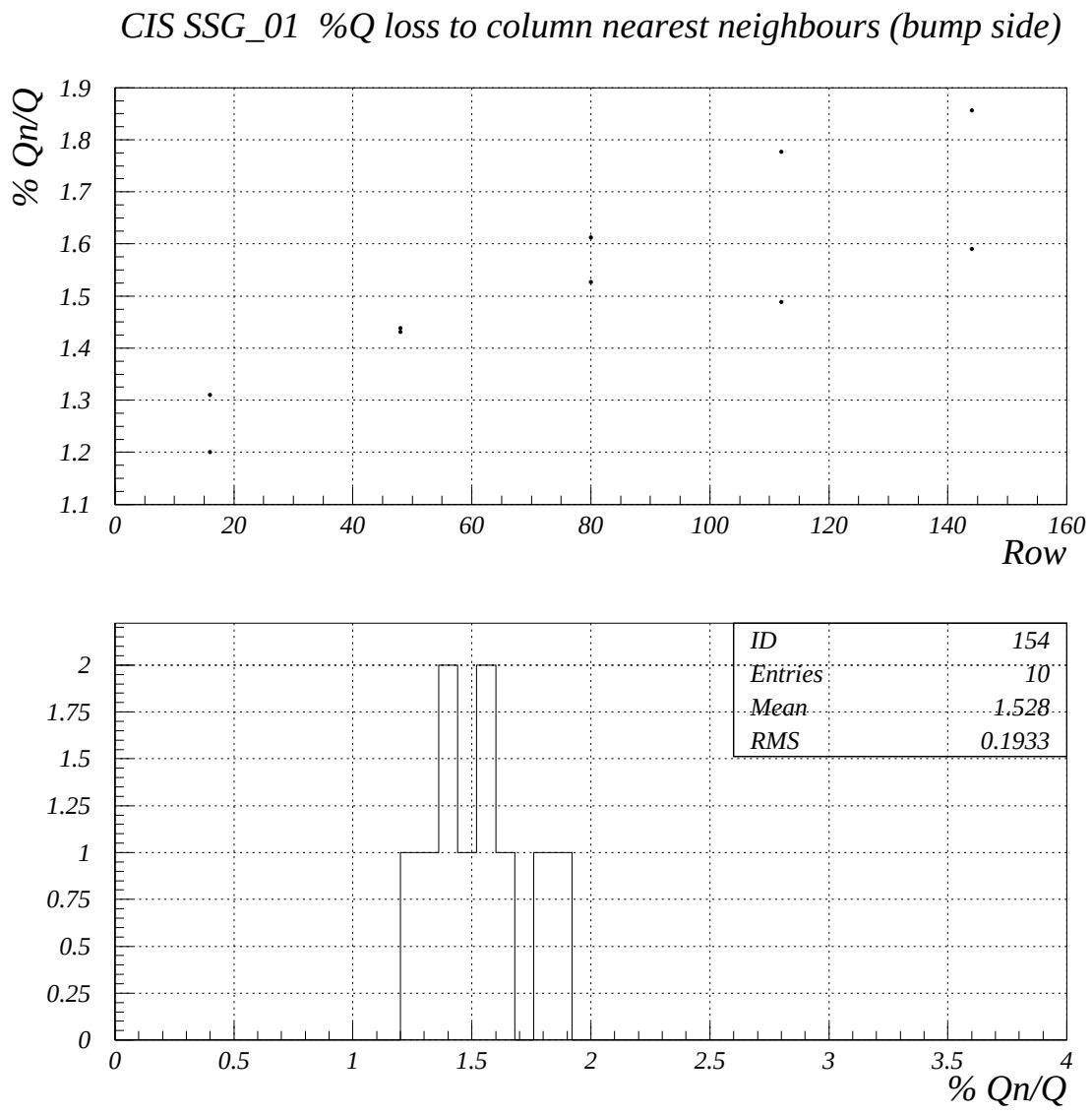
# For SSG (highest crosstalk) study other couplings:




- Crosstalk to row neighbors which are next to nearest (n+2 and n-2).
- Observed value is about 1.2%, compared to the nearest neighbor value of 2.3%

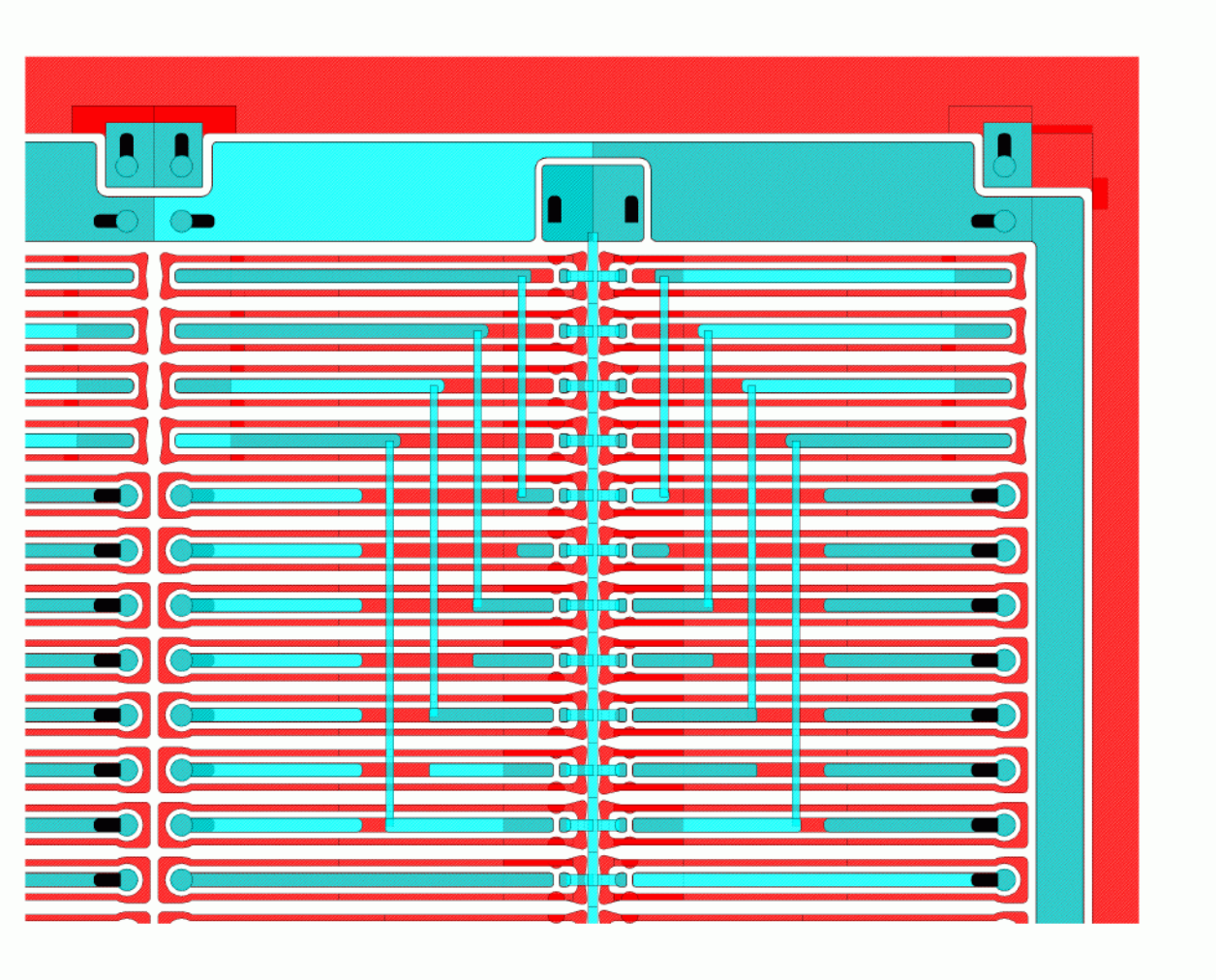
# For SSG (IZM bumps), study crosstalk between columns:



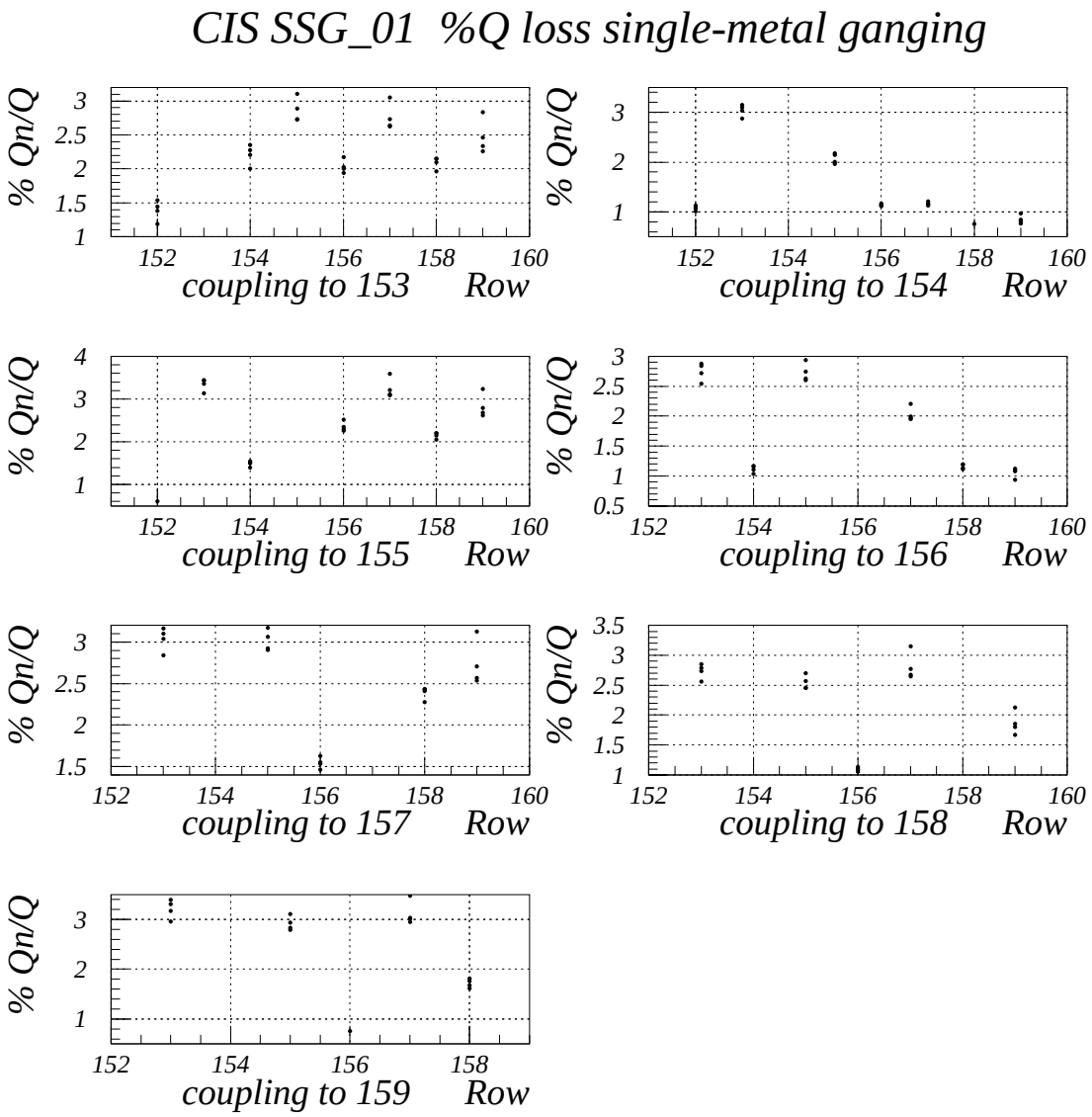

- Crosstalk to nearest neighbors in next column (but only when they are bump neighbors, for example column 1 and 2).
- Approximate value is 1.5%. A similar value is observed for the diagonal nearest neighbors in the next column.
- This would seem to be related to the inter-bump capacitance, but seems quite large for this source.
- A measurement on a Boeing Indium-bumped device gives a smaller value of about 0.6%, perhaps due to smaller bump size.

# Complex region at the top of each detector is special:

- In order to provide full coverage of regions on module between active die, four additional pixels are “ganged” together with pixels at the top of the column:
  - pixels 153,155,157,159 are “ganged” to an additional pixel beyond the active area.
  - This figure indicates the single-metal implementation
  - Because the metal traces cross all implants from 153 to 159, additional crosstalk would be expected.



# Study crosstalk between pixels in ganged region of single-metal ganged detector:




- Look at all possible couplings between eight topmost pixels, reading out all eight pixels each time.
- Find that coupling between ganged pixels (153, 155, 157, 159) is always about 3%, independent of distance involved.
- Coupling of ganged pixels to non-ganged pixels that are crossed by the ganging trace (153 to 154, 156 158) is about 2%
- Results very similar for double metal ganging.

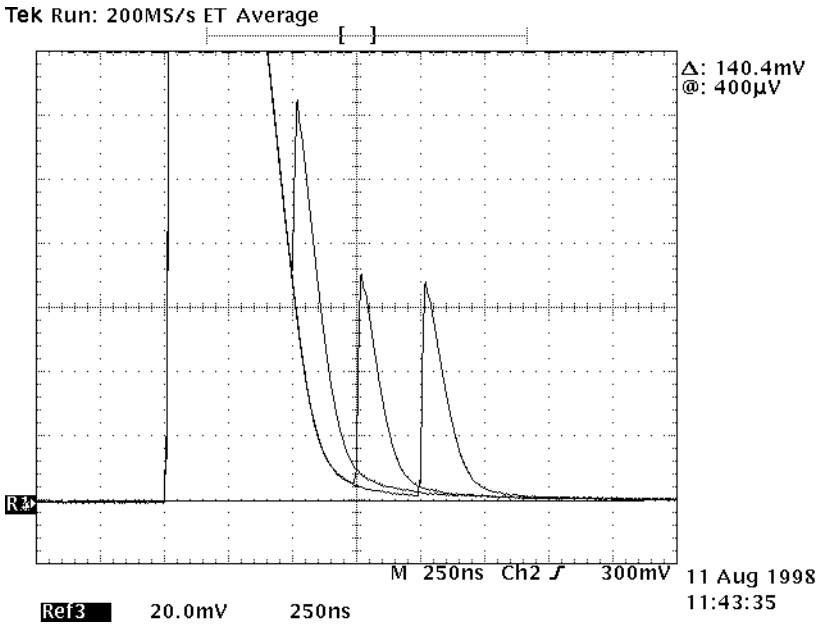
# Additional studies:

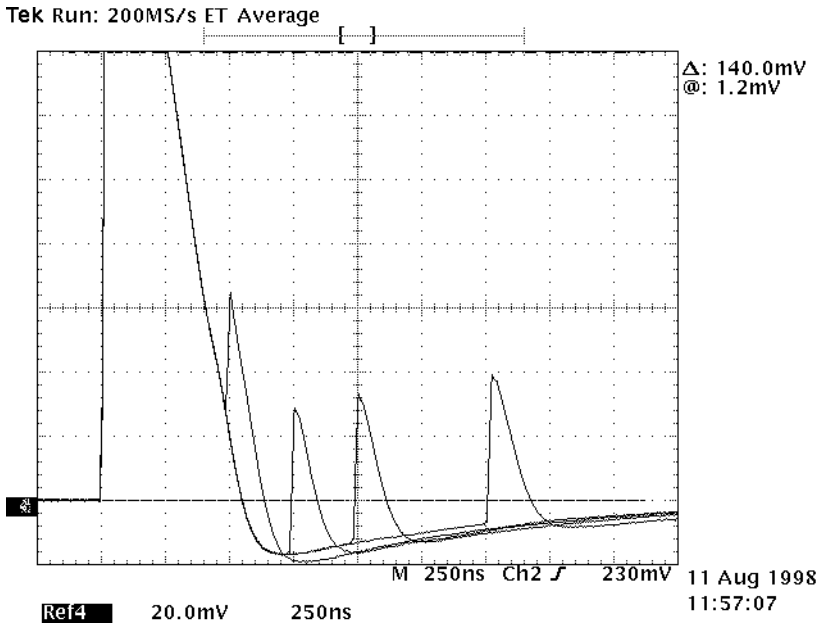
- Find crosstalk changes very little when FE bias is changed (FPDAC, CINDAC, or D1DAC).
- Have attempted to measure crosstalk as the difference in threshold between injecting one pixel, and injecting that pixel plus its two nearest neighbors. This requires taking the difference of two thresholds, but does not rely on the injection of very large charges to make the measurement. It is necessary to make measurements using the two techniques in a repetitive sequence to eliminate time variations. Even in this case, it is difficult to measure values at the 1% level. The measurements indicate that the crosstalk measured with this technique is slightly lower than that measured with the original method.

# Double Pulse Resolution

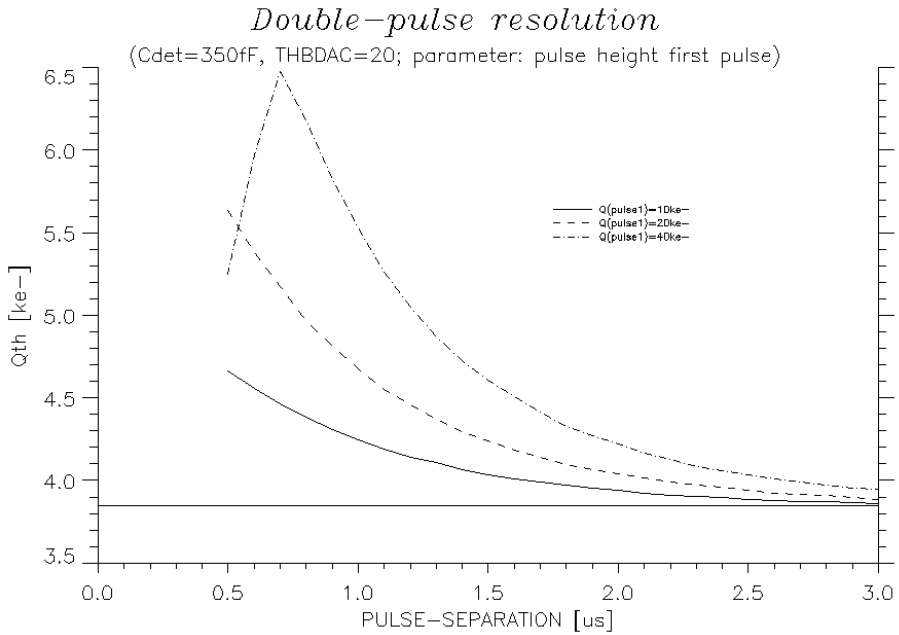
## Study response of front-end to second pulse as a function of amplitude and separation of pulses:

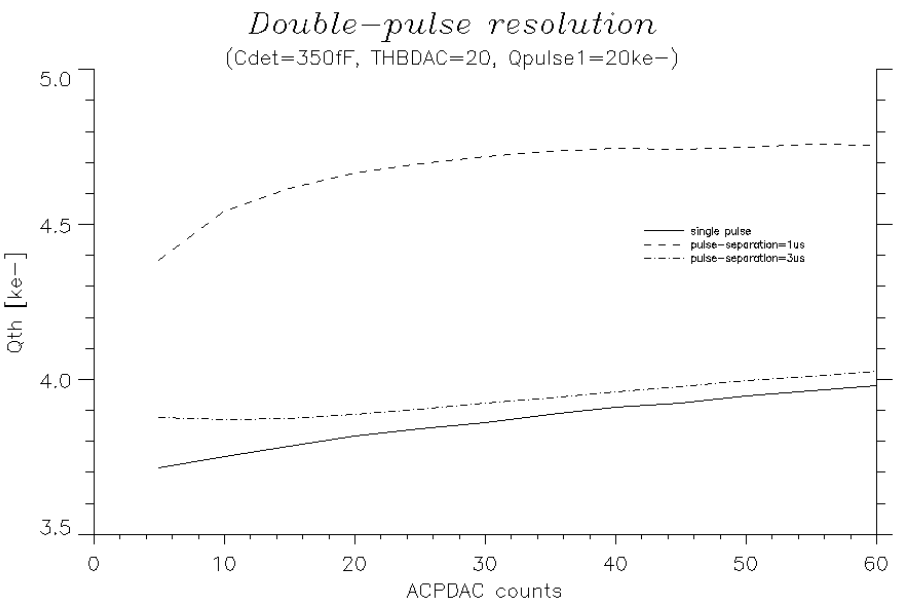
- Waveforms indicate that the preamplifier is very linear (left plot), and that the problems are introduced by the AC-coupling stage which introduces some small undershoot (right plot):



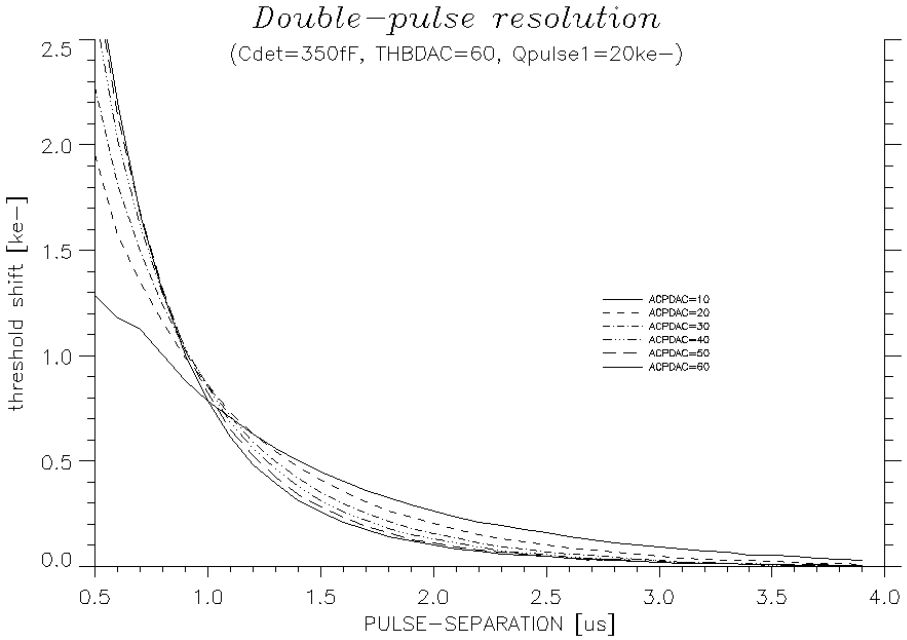
- Scan the separation between the two pulses, for three different input amplitudes, and look at the threshold for a second pulse (FPDAC=20):

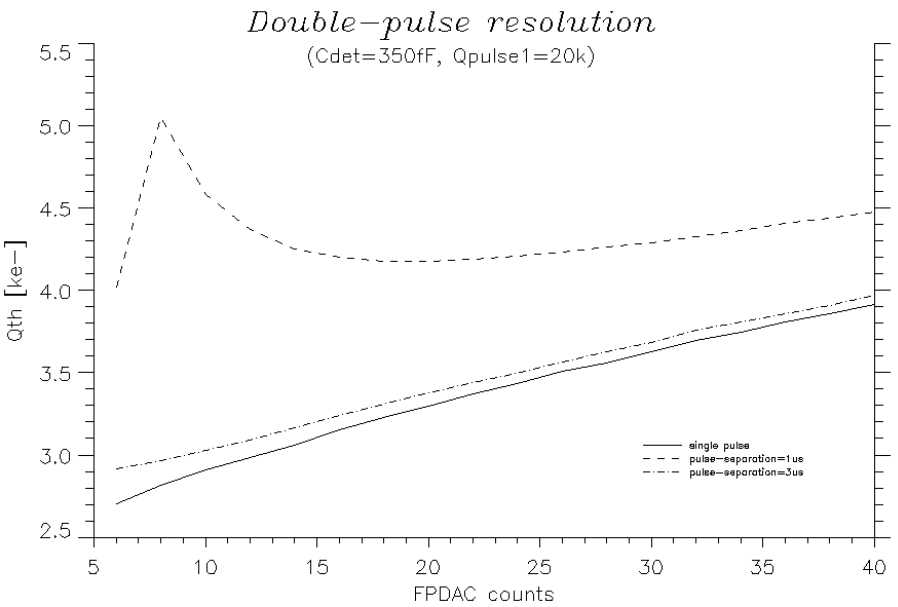



- For very large charge, see direct tail of input pulse. For smaller charges, see the undershoot of the AC-coupling stage.
- For a 20Ke input charge, the threshold shift is about 1Ke after about 1 µs, and negligible after 2 µs.
- The behavior of the threshold shift is not strongly influenced by the AC coupling bias (ACPDAC = ABSDAC).

- The shape of the AC-coupling transfer function is slightly changed by changing the ABSDAC value, with smaller values of ABSDAC preferred (default is typically taken as 20):



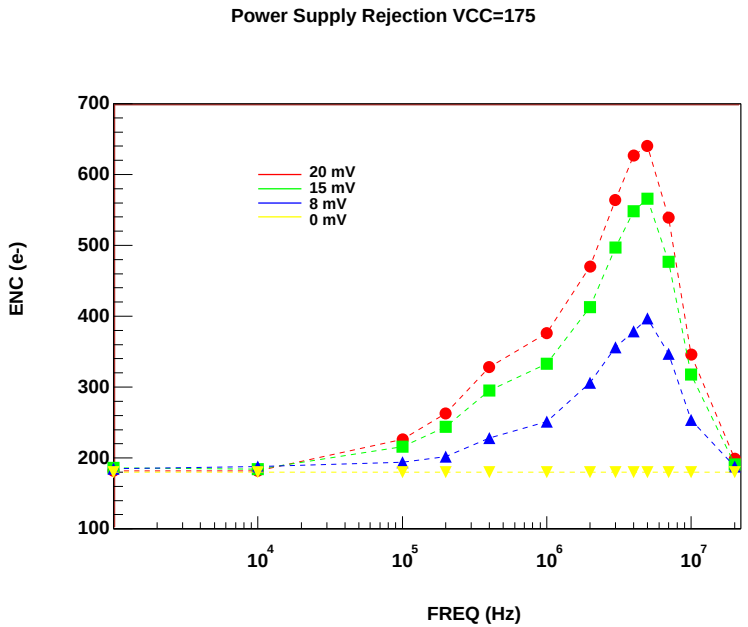



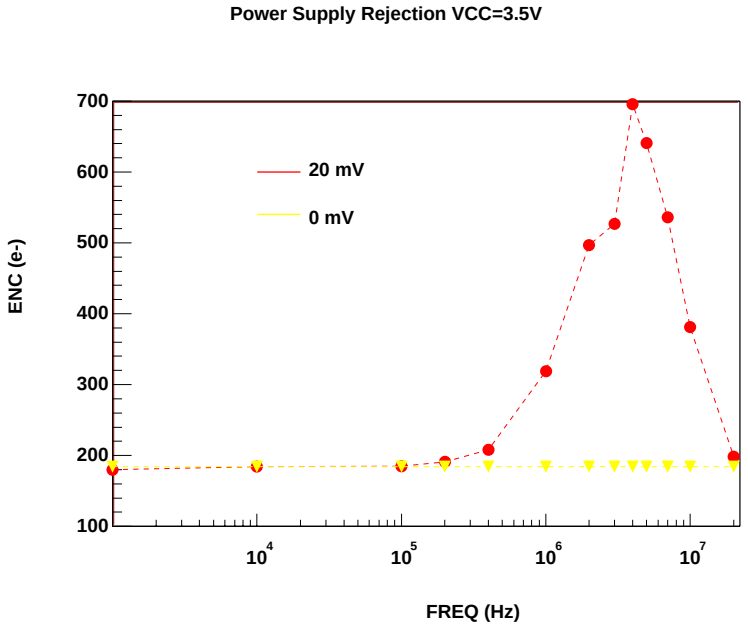

- The threshold shift is a function of FPDAC, simply due to the change in shaping time (return-to-baseline).
- The threshold shift is observed to be completely independent of threshold (THBDAC), indicating that the effect arises entirely in the AC-coupling stage.

# Power Supply Rejection Measurements

## Inject noise into different power supplies, and measure effect on noise level.

- Use test chip and measure noise level using threshold scan technique (not looking at preamp noise only, but effects on the complete system).
- Initial measurement made with FPDAC=20 and 350 fF load, giving about 180e.
- Drive chip supply directly with sine wave from low-impedance pulse generator.



# Implications of power supply rejection measurements:

- These measurements were made by removing the local decoupling capacitors from the test chip and driving the relevant power supply input directly with the waveform generator, and keeping the average DC level fixed. The noise is injected only on the supply and not on the return (ground).
- Charge is injected at about 10 KHz, and a scaler integrates the discriminator output for about 1 sec. Both of these frequencies are uncorrelated with the sine wave generator, hence the average power supply voltage is constant.
- Default DAC settings were used, including FPDAC=20.
- In the low frequency region (below 1 KHz) , it was possible to drive the chip with 1V or so of AC and see no significant performance degradation. Similarly, in the region of the LHC clock frequency, there is also no significant sensitivity.
- In the frequency range with highest gain (roughly 0.2-10 MHz), the chip has no rejection (100e noise observed for 1 mV RMS on supply). Power supply ripple in this region should be kept to the 1 mV RMS level in order to be negligible.
- It may be necessary to more carefully engineer the preamp-discriminator block so that its dependence on local supply voltage is minimized, and most sensitivity arises from variations in the bias currents supplied from the bottom of the column. The bias circuits then could be carefully engineered to reduce the sensitivity of the output current to the power supply voltage.

# Other measurements:

- It would be useful to make other measurements in which a fast risetime square wave with a low frequency is used to inject noise into the supplies and one looks for noise increases associated with the edges to study “spike sensitivity”.
- The present measurements should also be performed for a complete electronics plus detector assembly to check whether the effects are the same.

# Decoupling and Grounding Thoughts:

## Analog supplies:

- For reducing sensitivity in the high-gain region, multi-layer surface mount ceramics with values of about 0.1 μF should work, as the minimum in their impedance curve is in the 3-10 MHz region. Smaller values are not very effective in this frequency range, and larger values require quite large packages.
- For the two critical analog supplies, many capacitors may be necessary on a module, but perhaps not at every FE chip. Rating should be more than 6V.

## Digital supply:

- For the digital supply, the issues are different, since one is just trying to prevent current spikes from creating voltage spikes that could affect the operation of the digital circuitry. Here it may be more important to have smaller decoupling capacitors at every FE chip (say 0.01 μF).
- In addition, one would like to suppress any spikes in the digital supply/return before they propagate into the analog supply/return.

## HV supply:

- Here the decoupling capacitor also provides a local AC return path for the signal current. Values of many nF and ratings of 1 KV are probably required, with series resistor(s) to isolate the detector from the input supply.

# Lower frequency effects:

- For providing current during short periods (10's of μs) during which the current consumption of the FE chips may change significantly but the power supplies cannot follow, high quality Tantalum capacitors in the 10 μF range are needed (this will roughly cope with a $\Delta I = 0.1A$ for a period of 10 μs with a $\Delta V = 0.1V$).
- Switching supplies typically take several cycles of their switching frequency to respond to current surges. However, depending on whether and where sense lines are used, and whether there is processing in the supply to account for the $\Delta V$ on the cable, the time constants could get longer. This will cause problems for the supply filtering at the module, and could require local rad-tolerant regulators...
- Careful circuit design and engineering to minimize $\Delta I$ surges is very important. It is to be expected that there will be surges at the internal clock frequencies (10, 20, 40 MHz, ignoring the command decoder), and also surges associated with trigger processing and data transmission.

# Grounding and isolation:

- A critical issue is how and where to connect the different return paths for the supplies. In total, there will be DVdd, AVdd, AVcc, VDet, VPIN, and VLASER arriving at each module.
- Nominally, AVdd, AVcc, and VDet would be referenced to a local analog ground (they share current return paths and cannot be easily separated). AVdd and AVcc would share a common return to their supply, and VDet would have a separate return.
- The remaining supplies would be connected resistively together in a local ground (to avoid large $\Delta V$ between different “grounds”, and also avoid mixing current return paths for different supplies with different noise requirements). VPIN in particular is a sensitive supply.
- In principle, all returns at the supply end, with the possible exception of AVcc and AVdd, would have isolated grounds. It is expected that only the high current supplies (AVdd, AVcc, DVdd) would operate with remote sensing. This picture gets more complex if the supply modularity is two (two modules per LV supply).
- The above is complicated by the constraints imposed within the mixed mode IC’s themselves. It is difficult to implement independent current return paths for different supplies to the same electronics die, as they share substrate connections (these are capacitive connections in SOI processes). Careful layout, use of guard rings, etc. is required to isolate the different circuit sections.